An electronic device includes a trigonal crystal substrate defining a (0001) C-plane. The substrate may comprise Sapphire or other suitable material. A plurality of rhombohedrally aligned SiGe (111)-oriented crystals are disposed on the (0001) C-plane of the crystal substrate. A first region of material is disposed on the rhombohedrally aligned SiGe layer. The first region comprises an intrinsic or doped Si, Ge, or SiGe layer. The first region can be layered between two secondary regions comprising n+doped SiGe or n+doped Ge, whereby the first region collects electrons from the two secondary regions.

4 Claims, 7 Drawing Sheets
References Cited

U.S. PATENT DOCUMENTS


OTHER PUBLICATIONS


* cited by examiner
Fig. 1

Layer

○ Holes, positive charge carrier

★ Electrons, negative charge carrier

Ge Si Ge Si Ge

Conduction Band

Valence Band

Energy
Fig. 2

- **p + Si/SiGe Capping layer**
- **p+ doped SiGe (Region-I)**
- **Intrinsic or p- doped Ge (Region-II)**
- **p+ doped SiGe (Region-I)**
- **Intrinsic or p- doped Ge (Region-II)**
- **p+ doped SiGe (Region-I)**
- **Intrinsic or p- doped Ge (Region-II)**
- **p+ doped SiGe (Region-I)**
- **Rhombohedral SiGe buffer**
- **Trigonal Substrate**

- **Holes, positive charge carrier**
- **Ionized p-dopants, negatively charged coulomb scattering center**
Fig. 3

- n+Ge/SiGe Capping layer
- n+ doped SiGe (Region-I)
- Intrinsic or n- doped Si (Region-II)
- n+ doped SiGe (Region-I)
- Intrinsic or n- doped Si (Region-II)
- n+ doped SiGe (Region-I)
- Intrinsic or n- doped Si (Region-II)
- n+ doped SiGe (Region-I)
- Rhombohedral SiGe buffer
- Trigonal Substrate

- Electrons, negative charge carrier
- Ionized n-dopants, positively charged coulomb scattering center
Fig. 4

Mobility (cm²/Vs) vs. Acceptor density (/cm³)

Fig. 5

Mobility (cm²/Vs) vs. Donor density (/cm³)
Fig. 6

- Light (1)
  - Capping layer
  - Intrinsic or p-doped SiGe (Region-V)
  - Intrinsic or p-doped pure Ge (Region-IV)
  - Intrinsic SiGe (Region-III)
  - Intrinsic or n-doped pure Si (Region-II)
  - Intrinsic or n-doped SiGe (Region-I)
  - Rhombohedral SiGe buffer
  - Trigonal Substrate

- Light (2)

- Holes, positive charge carrier
- Electrons, negative charge carrier
- Ionized n-dopants, positively charged coulomb scattering center
- Ionized p-dopants, negatively charged coulomb scattering center
Holes, positive charge carrier
Electrons, negative charge carrier
Ionized n-dopants, positively charged coulomb scattering center
Ionized p-dopants, negatively charged coulomb scattering center
1
HIGH MOBILITY TRANSPORT LAYER STRUCTURES FOR RHOMBOHEDRAL SI/GE/SIGE DEVICES

CROSS-REFERENCE TO RELATED PATENT APPLICATION(S)

This patent application claims the benefit of and priority to U.S. Provisional Patent Application No. 61/779,317, filed on Mar. 13, 2013, the contents of which are hereby incorporated by reference in their entirety.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

The invention described herein was made in the performance of work under a NASA contract and by employees of the United States Government and is subject to the provisions of Public Law 96-517 (35 U.S.C. §202) and may be manufactured and used by or for the Government for governmental purposes without the payment of any royalties thereon or therefore. In accordance with 35 U.S.C. §202, the contractor elected not to retain title.

FIELD OF THE INVENTION

The present invention relates to integrated circuits ("IC") semiconductor electronic devices, and in particular to an electronic device including a high mobility transport layer such as crystalline SiGe on a sapphire chip.

BACKGROUND OF THE INVENTION

Performance of many electronic devices, such as transistors, solar cells, thermo-electric (TE) devices can be improved if carrier mobility is increased. Prior calculations show that Si and Ge have Type-I band gap alignment in cubically strained and relaxed layers. Quantum wells and superlattices with Si, Ge, and SiGe have been good noble structures to build high electron mobility layers and high hole mobility layers. However, the atomic lattice constant of Ge is bigger than that of Si, and direct epitaxial growth generates a high density of misfit dislocations which decreases carrier mobility and shortens the life time of devices. Known configurations utilize special buffer layers such as super lattice or gradient indexed layers to grow Ge on Si wafers or Si on Ge wafers. The growth of these buffer layers takes extra time and effort. For example, the layers can be subject to a post-annealing process to remove dislocations by dislocation gliding inside of the buffer layer or layers.

BRIEF SUMMARY OF THE INVENTION

Prior Silicon-on-Sapphire (SOS) technology typically utilizes R-plane (1-102) Sapphire which has a rectangular plane. Silcon (100) crystal is grown on the R-plane Sapphire. In contrast, the present invention utilizes C-plane (0001) Sapphire which has a triangle plane and a Si (Ge) (C) (111) or an alloy of group IV semiconductor (111) crystal is grown thereon.

One embodiment is an electronic device including a trigonal crystal (e.g. Sapphire) substrate defining a (0001) C-plane, and plurality of rhombohedrally aligned (111)-oriented crystals disposed on the (0001) C-plane of the Sapphire substrate. The (111)-oriented crystals can comprise a group IV semiconductor or an alloy of group IV semiconductors (e.g. SiGe). The device further includes a first region disposed on the rhombohedrally aligned SiGe layer, the first region comprising a layer of intrinsic or doped Si, Ge, SiGe. The first region can comprise p-doped Ge or intrinsic Ge, wherein the first region has a thickness of less than about 100 nanometers ("nm"). The first region can be layered between two adjacent secondary regions, the secondary regions can comprise p+ doped SiGe or p doped Si, such that the first region collects holes from the secondary regions. The first region can have at least two times higher hole mobility than the adjacent secondary regions.

The first region can comprise n-doped Si or intrinsic Si, wherein the first region has a thickness that is less than about 100 nm. The first region can be layered between two adjacent secondary regions, wherein the secondary regions comprise n+ doped SiGe or Ge, such that the first region collects electrons from the two adjacent secondary regions. The first region can have at least two times higher electron mobility than the adjacent secondary regions.

Another embodiment is a method of fabricating an electronic device. The method includes providing a trigonal crystal substrate defining a (0001) C-plane. Heat is applied to the substrate to raise the temperature of the substrate to a level that facilitates growth of rhombohedrally aligned Si or SiGe material. A layer of a buffer material selected from the group consisting of group IV semiconductors and alloys of group IV semiconductors is grown on the substrate. The first region comprises p doped Ge or intrinsic Ge, wherein the first region has a thickness of less than about 100 nm. The first region may be layered between two adjacent fourth regions comprising n+ doped SiGe or Ge such that the first region collects electrons from the two fourth regions. The first region can have at least two times higher hole mobility than the adjacent secondary regions, and the third region can have at least two times higher electron mobility than the adjacent fourth regions.

This invention will be further understood and appreciated by those skilled in the art by reference to the following specification, claims, and appended drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram that shows a Type-II bandgap alignment of Si and Ge;

FIG. 2 is a schematic diagram that shows rhombohedral SiGe/Ge high hole mobility layers for p-type TE material, transistor, and solar cell layer.
FIG. 3 is a schematic diagram that shows a rhombohedral SiGe/Si high electron mobility layers for n-type TE material, transistor, and solar cell layer;

FIG. 4 is a graph that shows an approximation of hole mobility vs. hole density of p-type Ge;

FIG. 5 is a graph that shows an approximation of electron mobility vs. donor density of n-type Si;

FIG. 6 is a schematic diagram that shows an enhanced solar cell structure-I with two high mobility transport layers made of electron quantum well and hole quantum well;

FIG. 7 is a schematic diagram that shows an enhanced solar cell structure-II with high mobility transport layers made of electron quantum well and hole quantum well;

FIG. 8 is a flowchart showing fabrication of a device according to one embodiment of the present invention.

DETAILED DESCRIPTION

For purposes of description herein, the terms “upper,” “lower,” “right,” “left,” “rear,” “front,” “vertical,” “horizontal,” and derivatives thereof shall be related to the invention as oriented in FIG. 2. However, it is to be understood that the invention may assume various alternative orientations, except where expressly specified to the contrary. It is also to be understood that the specific devices and processes illustrated in the attached drawings, and as described in the following specification are simply exemplary embodiments of the inventive concepts defined in the appended claims. Furthermore, references to specific items or features shall not be construed as limiting the item or feature to one-piece or multi-piece items or features. Hence, specific dimensions and other physical characteristics relating to the embodiments disclosed herein are not to be considered as limiting, unless the claims expressly state otherwise.

As discussed above, carrier mobility affects performance of many electronic devices such as transistors, solar cells, thermo-electric (TE) devices and the like. The performance of such devices can be improved if carrier mobility is increased. Prior calculations show that Si and Ge have similar band alignment in cubically strained and relaxed layers.

The present disclosure relates to fabrication of more complex high mobility layer structures for rhombohedrally aligned SiGe on a trigonal substrate. It will be understood that other group IV semiconductors and alloys may be rhombohedrally aligned on a trigonal substrate. Thus, according to other embodiments, Si, Ge, C, SiC, GeC, and SiGeC can also be utilized to form a rhombohedrally aligned buffer layer or a trigonal substrate. The trigonal substrate can comprise Sapphire, Lithium Niobate (LiNbO₃), Langsite, Langatate, Antimony, Calcite, or other suitable material.

FIG. 1 is a Si layer disposed between two Ge layers. The Si layer has a slower conduction band that forms a quantum well for electrons. In other words, electrons in the conduction band drift into the Si layer to “find” a lower energy state. Also, a Ge layer between two Si layers has a higher valence band top energy level such that it forms a quantum well for holes (i.e. it attracts holes in the valence band). This principle concept is utilized in the high mobility transport layer structures in FIGS. 2 and 3 according to one embodiment.

In FIG. 2, a Si layer is dispersed on a trigonal substrate. An optional rhombohedral Si buffer layer can be formed on a trigonal substrate. The trigonal substrate can comprise Sapphire or other suitable material. In FIG. 2, the circles with vertical lines in them represent ionized p-dopants, or negatively charged Coulomb scattering centers. The open dots/circles represent holes or positive charge carriers, Region-I is a highly doped p-type SiGe (p-doped SiGe) and Region-II is intrinsic or low-density doped p-type pure Ge layer (no Si). Region-I has a higher valence band top energy level such that it forms a quantum well for holes (i.e. it attracts holes in the valence band). This principle concept is utilized in the high mobility transport layer structures in FIGS. 2 and 3 according to one embodiment.

FIG. 3 shows the type-II bandgap alignment of Si and Ge such that Si has a lower conduction band energy and a lower valence band energy than Ge. The bandgap of Si is 1.1 eV and that of Ge is 0.67 eV at 300 °C. Therefore, a new calculation of bandgap energy is required because the strain direction of the rhombohedrally aligned SiGe is not the same as that of cubically strained and relaxed Si/Ge/SiGe. Therefore, a new calculation of bandgap alignment is needed for strain effects on [111] direction which are perpendicular to <2-20> in-plane directions.

In FIG. 3, a SiGe and Ge layers are grown with rhombohedral alignment on trigonal substrate. An optional rhombohedral Si buffer layer can be formed on a trigonal substrate. The trigonal substrate can comprise Sapphire or other suitable material. In FIG. 2, the circles with vertical lines in them represent ionized p-dopants, or negatively charged Coulomb scattering centers. The open dots/circles represent holes or positive charge carriers, Region-I is a highly doped p-type SiGe (p-doped SiGe) and Region-II is intrinsic or low-density doped p-type pure Ge layer (no Si). Region-I has a higher valence band top energy level such that it forms a quantum well for holes (i.e. it attracts holes in the valence band). This principle concept is utilized in the high mobility transport layer structures in FIGS. 2 and 3 according to one embodiment.
2000 cm²/V·s at 10¹⁹/cm³ doping density. Therefore 10 times faster mobility is achieved with high mobility hole transport layer in FIG. 2.

FIG. 3 shows a similar high mobility transport layer for electrons comprising a heavily doped n-Ge layer (Region-I) and an intrinsic or low n-type doped pure Si (no Ge) layer (Region-II). In FIG. 3, the circles with vertical lines in them represent ionized p-dopants, or negatively charged Coulomb scattering centers. The open dots/circles represent holes or positive charge carriers. Intrinsic or low n-doped Si layer (Region-II) has a lower conduction band than that of SiGe or Ge in Region-I, so that Region-II forms a quantum well for electrons. Similarly, the mobile electrons from heavily doped Region-I (n-SiGe) drift into electron quantum well of Region-II which has greater mobility with very few scattering centers. Therefore Region-II (intrinsic or low n-doped Si) layer becomes super highway of mobile electrons, i.e., a high mobility electron-transport layer.

According to another example, Region-I (Ge or SiGe) can be doped with n-type dopants such as Phosphorous of 10¹⁹/cm³ concentration, and Region-II (pure Si) may be low density n-type doped at 10¹⁶/cm³ concentration. FIG. 5 shows the enhancement of electron mobility from 120 cm²/V·s at 10¹⁹/cm³ doping density to 1200 cm²/V·s at 10¹⁶/cm³ doping density. Therefore 10 times faster mobility is achieved with the high mobility electron transport layer in FIG. 3.

In the examples of high mobility transport layers above, the ultra fast Region-II is pure Ge (no Si) and pure Si (no Ge) in FIGS. 2 and 3, respectively. Thus, the fast transport layers do not have an alloy scattering effect and also maintain high mobility of intrinsic or very low doped semiconductors. Repetition of Region-I and Region-II in a device or structure generates a plurality of high mobility transport layers making high current flow possible.

An optional Rhombohedral SiGe buffer layer can be utilized to improve the single crystalline quality of Region-I and Region-II. An optional capping layer can be utilized to reduce surface charge loss effect.

The high mobility transport layer structures in FIGS. 2 and 3 can be used for many electronic device applications. For example, if the left side is hot (above 500°C) and right side is cold (300°C), this structure can be used as a p-type TE material structure (FIG. 2 structure) and a n-type TE material structure (FIG. 3 structure). Compared to conventional TE devices, this arrangement provides higher current output and better figure of merit (thermoelectric ZT factor) due to the increased charge-carrier mobilities. Similar structures with one or more multiples of Region-I and Region-II layers under gate voltage can be used for transistors. Also, the structures of FIG. 2 or 3 can be utilized in solar cells. Such solar cells have higher efficiency due to the enhanced charge transport mechanism of the high mobility transport layers.

With further reference to FIGS. 6 and 7, enhanced solar cell structures can be fabricated by integrating electron quantum well of pure Si layer and hole quantum well of pure Ge layer together.

Region-I is intrinsic or moderately n-type doped SiGe which generates free electrons upon light injection and Region-II is intrinsic or low n-type doped pure Si layer as an electron quantum well (QW) for high mobility transport layer. Region-III is an optional intrinsic SiGe layer that separates two high mobility electron-electron transport layers, electron quantum well and hole quantum well. Region-III also generates and provides electrons and holes into Region-II (electron QW) and Region-IV (hole QW) upon light injection. Region IV is made with intrinsic or low p-type doped pure Ge (no Si) layer as hole QW for high mobility hole transport layer. Region-V is intrinsic or moderately p-type doped SiGe layer that generates and provides mobile holes into Region-IV (hole QW).

An optional capping layer reduces charge carrier loss into the semiconductor surface and an optional rhombohedral SiGe buffer layer improves single crystalline quality of Region-I to Region-V. The light injection can be from above the surface “Light(1)” or form backside through transparent trigonal substrate “Light(2).” Many trigonal substrates such as Sapphire are transparent in the solar spectrum. Therefore, backside illumination can be made through transparent trigonal substrate. This arrangement has advantages, including (1) metal electrodes can be deposited on the front side without forming shadows; and (2) additional patterning and etching can be formed on the backside of a transparent trigonal substrate to absorb more direct sun light or ambient environmental light. FIG. 7 shows another similar structure as that of FIG. 6.

The enhanced solar cell structures in FIGS. 6 and 7 can be applied to not only rhombohedral SiGe/SiGe structures on trigonal substrates, but also conventional cubic SiGe/SiGe structures on square (100) planes of cubic substrates. The high mobility electron and hole transport layers are separately connected to (-) and (+) metal electrodes by ohmic contact and deliver more photo-voltaic current than conventional solar cells.

With reference, to FIG. 8, a process of fabricating a multi-layer hybrid structure 30 includes providing a C-plane Sapphire wafer 15 at step 50. Processes for fabricating C-plane Sapphire wafers are known, such that step 50 will not be described in detail. An optional heat absorption layer 52 such as Carbon (C) or Titanium (Ti) can be deposited on one side of the Sapphire wafer 15 at step 55 utilizing a suitable known process. A substrate heater 54 is utilized to apply IR heat 53 to raise the temperature of the Sapphire layer 15 to the optimum growth temperature for rhombohedral aligned Si/SiGe on C-plane Sapphire. The optional heat absorbing layer 52 absorbs more IR heat 53 and assists in maintaining a uniform high substrate temperature. It will be understood that other heating methods and processes can also be utilized.

At step 60, Si/SiGe layers 10 are grown on the back side of the Sapphire wafer 15 utilizing a known epitaxial growth method. Examples of such processes include sputtering, MBD, MOCD, PVE, HVPE, e-Beam deposit, LPE, LPCD, etc. Optional Si/SiGe device pre-fabrication processes such as chemical-mechanical polishing (CMP), dopant drive-in, ion-implantation, and other such processes can optionally be performed at step 65. Deposition or growth of a protection layer 72 is performed at step 70. Layer 72 protects the Si/SiGe layer 10 during formation of the III-Nitride structures.

In step 75, the optional heat absorbing layer 52 is removed (if necessary) utilizing a suitable known etching process such as wet etching, dry etching, plasma etching, reactive, on etching, or the like to form an exposed Sapphire surface 76. Then, at step 80, heat 82 is applied and III-Nitride layers 20 such as GaN, AlN, AlGan, and InN are grown on the exposed surface 76 of front side 18 of C-plane Sapphire (opposite side from Si/SiGe layers). III-Nitride processes are known in the art, and this step in the process will not therefore be described in detail. Known III-Nitride pre-device fabrication processes such as chemical-mechanical polishing (CMP), dopant ion-implantation, and etc. can be performed in step 85. In step 90, a second protection layer 92 (such as silicon oxide or silicon nitride) is deposited or
The hybrid wafer product can be further processed by removing and depositing each protection layer at a time and performing further post-wafer device fabrication steps as described above. Growth of the Si/SiGe and III-Nitrides during the process illustrated in FIG. 8 can be adjusted utilizing x-ray diffraction methods as described in U.S. Pat. Nos. 7,769,135 and 7,558,371. Use of these x-ray diffraction methods provides quality control and permits the optimum growth parameters for forming hybrid crystals with more than 99% single crystallinity. These x-ray diffraction methods permit measuring the single crystal versus twin defect ratio in full wafer scale.

It will be understood that the principles and processes described above can also be utilized with SiGeC alloy in addition to SiGe alloy on C-plane sapphire. Si, Ge, and C are group IV semiconductor materials that can readily build the rhombohedral double side structure with GaN in a substantially similar epitaxy. All cited patents, patent applications, and other references are incorporated herein by reference in their entirety. However, if a term in the present application contradicts or conflicts with a term in the incorporated reference, the term from the present application takes precedence over the conflicting term from the incorporated reference.

All ranges disclosed herein are inclusive of the endpoints, and the endpoints are independently combinable with each other. Each range disclosed herein constitutes a disclosure of any point or sub-range lying within the disclosed range.

The use of the terms “a” and “an” and “the” and similar referents in the context of describing the invention (especially in the context of the following claims) are to be construed to cover both the singular and the plural, unless otherwise indicated herein or clearly contradicted by context. “Or” means “and/or.” As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items. As also used herein, the term “combinations thereof” includes combinations having at least one of the associated listed items, wherein the combination can further include additional, like non-listed items.

Reference throughout the specification to “another embodiment”, “an embodiment”, “some embodiments”, and so forth, means that a particular element (e.g., feature, structure, and/or characteristic) described in connection with the embodiment is included in at least one embodiment described herein, and can or cannot be present in other embodiments. In addition, it is to be understood that the described elements can be combined in any suitable manner in the various embodiments and are not limited to the specific combination in which they are discussed.

This written description uses examples to disclose the invention, including the best mode, and also to enable anyone skilled in the art to make and use the invention. The patentable scope of the invention is defined by the claims, and includes other examples that occur to those skilled in the art. Such other examples are intended to be within the scope of the claims if they have structural elements that do not differ from the literal language of the claims, or if they include equivalent structural elements with insubstantial differences from the literal language of the claims.

The invention claimed is:

1. An electronic device, comprising:
   a trigonal crystal substrate defining a (0001) C-plane;
   a rhombohedrally aligned buffer layer comprising a plurality of rhombohedrally aligned (111)-oriented crystals disposed on the (0001) C-plane of the crystal substrate, wherein the plurality of rhombohedrally aligned (111)-oriented crystals comprise a material selected from the group consisting of group IV semiconductors and alloys of group IV semiconductors; and
   at least one layer comprising a first region disposed on the rhombohedrally aligned buffer layer, the first region comprising a p-doped SiGe layer having a thickness of less than about 100 nm and a secondary region disposed on the first region, the secondary region comprising a p-doped Ge, or intrinsic Ge material to form a quantum well structure for the fast transport of holes, such that the secondary region collects holes from the first region; and
   wherein additional layers have the first region disposed on the secondary region and the secondary region disposed on the first region.

2. The device of claim 1, wherein the secondary region has at least two times higher hole mobility than the adjacent first region.

3. The device of claim 1, wherein the trigonal crystal substrate comprises a Sapphire material.

4. The device of claim 1, wherein the rhombohedrally aligned (111)-oriented crystals comprise a group IV semiconductor material. * * * * *