NEPP Update of Independent Single Event Upset Field Programmable Gate Array Testing

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Outline

- FPGA test guidelines
- Microsemi RTG4 heavy-ion results.
- Xilinx Kintex-UltraScale heavy-ion results.
- Xilinx UltraScale+ single event effect (SEE) test plans.
- Development of a new methodology for characterizing SEU system response.
- NEPP involvement with FPGA security and trust.
NEPP – Processors, Systems on a Chip (SOC), and Field Programmable Gate Arrays (FPGAs)

Best Practices and Guidelines

State of the Art COTS Processors
- Sub 32nm CMOS, FinFETs, etc
- Samsung, Intel, AMD

“Space” FPGAs
- Microsemi RTG4
- Xilinx MPSOC+
- ESA Brave (future)
- “Trusted” FPGA (future)

Graphics Processor Units (GPUs)
- Intel, AMD, Nvidia
- Enabling data processing

Radiation Hardened Processor Evaluation
- BAE
- Vorago (microcontrollers)

COTS FPGAs
- Xilinx Kintex+
- Mitigation evaluation
- TBD: Microsemi PolarFire

Partnering
- Processors: Navy Crane, BAE/NRO-
- FPGAs: AF, Aerospace, SNL, LANL, BYU,...
- Microsemi, Xilinx, Synopsis
- Cubic Aerospace

Potential future task areas:

artificial intelligence (AI) hardware, Intel Stratix 10

To be presented by Melanie Berg at the NASA Electronics Parts and Packaging (NEPP) Electronics Technology Workshop (ETW), Greenbelt, MD, June 26–29, 2017
FPGA SEU Test Guidelines

• Impact to community:
  – Currently it is difficult to compare device under test (DUT) test data because of differences in test vehicle and test methodology
  – The FPGA SEU Test Guidelines Document creates standardized test methodologies and provide a means for data comparison across organizations and FPGA types.
  – The FPGA SEU Test Guidelines Document points out best practices for DUT test structures, monitoring DUT functional response, visibility in DUT operation, DUT control, and DUT power.

• Update of the test guidelines will be available by December 2017.
  – Additional test structures.
  – Embedded processor testing techniques.

Various Triple Modular Redundant (TMR) Schemes Implemented in FPGA Devices

Block diagram of block TMR (BTMR): a complex function containing combinatorial logic (CL) and flip-flops (DFFs) is triplicated as three black boxes; majority voters are placed at the outputs of the triplet.

Block diagram of local TMR (LTMR): only flip-flops (DFFs) are triplicated and data paths stay singular; voters are brought into the design and placed in front of the DFFs.

Block Diagram of distributed TMR (DTMR): the entire design is triplicated except for the global routes (e.g., clocks); voters are brought into the design and placed after the flip-flops (DFFs). DTMR masks and corrects most single event upsets (SEUs).

TMR can be embedded in the FPGA or user inserted.
Impact to Community
Microsemi RTG4 FPGA

- Next generation to the space-grade Microsemi RTAXs.
- I/O interfaces are significantly more robust versus prior Microsemi space-grade FPGAs devices.
- Embedded mitigation, packaging, and qualification process makes this device space-grade.
- Flash based configuration – hence configuration is essentially SEU immune.
- Embedded flip-flop (DFF) SEU hardening.

**NEPP performs an independent study to determine the level of SEU susceptibility for the various RTG4 components.**
Microsemi RTG4: Device Under Test (DUT) Details

- New Entry into the Aerospace Market with Space-grade Expectation.
  - Bulk UMC 65nm CMOS process with an epitaxial layer. Flash based configuration.
  - Qualified to MIL-STD-883 Class B, and Microsemi will seek QML Class Q and Class V qualification.
- The DUT: RT4G150-CG1657M.
- We tested Rev B and Rev C devices.
- The DUT contains:
  - 158214 look up tables (4-input LUTs);
  - 158214 flip-flops (DFFs); 720 user I/O;
  - 210K Micro-SRAM (uSRAM) bits;
  - 209 18Kblocks of Large-SRAM (LSRAM);
  - 462 Math logic blocks (DSP Blocks);
  - 8 PLLs; and 48 global routes (radiation-hardened global routes);

LUT: look up table.
SRAM: sequential random access memory.
DSP: digital signal processing.
PLL: phase locked loop.
Microsemi RTG4: Device Under Test (DUT)
Embedded Hardening

DFFs are radiation hardened using LTMR and SET filters placed at the DFF data input.

Hardened configuration flash cell
Microsemi RTG4 Study Objectives

- This is an independent investigation that evaluates the single event destructive and transient susceptibility of the Microsemi RTG4 device.
- Design/Device susceptibility is determined by monitoring the DUT for Single Event Transient (SET) and Single Event Upset (SEU) induced faults by exposing the DUT to a heavy ion beam.
- Potential Single Event Latch-up (SEL) is checked throughout heavy-ion testing by monitoring device current.
- The objectives of this study are the following:
  - Analyze flip-flop (DFF) behavior in simple designs such as shift registers. Compare SEU behavior to more complex designs such as counters and finite impulse response (FIR) filters. Evaluating data trends helps in extrapolating test data to actual designs.
  - Analyze global route behavior – clocks, resets.
  - Analyze configuration susceptibility.
DUT Preparation

Top Side of DUT

- NEPP has populated two Rev B and four populated Rev C boards with RT4G150-CG1657M devices.
- The parts (DUTs) were thinned using mechanical etching via an Ultra Tec ASAP-1 device preparation system.
- The parts have been successfully thinned to 70um – 90um.

Bottom Side of DUT
Challenges for Testing

- Software is new… place and route is not optimal yet. Hence, it is difficult to get high speed without manual placement.
- Microsemi reports that devices show TID tolerance up to 160Krad.
  - Although, when testing with heavy-ions, dose tolerance will be much higher.
  - TID limits the amount of testing per device.
  - Number of devices are expensive and are limited for radiation testing.
  - A large number of tests are required.
- We will always need more parts.
- Current consortium participants:
  - NEPP (Goddard and JPL),
  - Aerospace Corporation, and
  - Microsemi.

TID: total ionizing dose
Test Setup

Labview GUI Connected to Memory Processing in HSDT. Commands are also sent (and echoed) to the HSDT through this RS232 interface.

Labview GUI connected to WSR or Counter Processing

Logic Analyzer Connected to WSR or Counter Outputs

CLK_SR_A

SHFT_CLK

DUT INPUTS

RTG4 DUT

DUT Outputs

TX232(1)

TX232(2)

RS232(1)

DUT Controls

General Tester Hardware

HIGH SPEED DIGITAL TESTER

Data Processing

CLK

RESET
# Microsemi RTG4 Designs Tested

<table>
<thead>
<tr>
<th>Test Structure</th>
<th>Frequency Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Global routes</td>
<td>2KHz – 150MHz</td>
</tr>
<tr>
<td>Shift Registers (WSRs)</td>
<td>2KHz – 150MHz</td>
</tr>
<tr>
<td>Counters</td>
<td>5MHz – 100MHz</td>
</tr>
<tr>
<td>Finite impulse response filters (FIRs). Math-block (DSP) testing</td>
<td>1MHz-100MHz</td>
</tr>
<tr>
<td>Embedded SRAM</td>
<td>N/A</td>
</tr>
</tbody>
</table>

*Test structures selected in order to investigate specific RTG4 components and data trends across a variety of designs.*
Windowed Shift Registers (WSRs): Test Structure

N levels of Inverters between DFF stages: 
N = 0, 8, and 18

DFF = D flip flop
4-bit Window Output

Shift Register Chain

$dly_{WSR_{8}} > dly_{WSR_{0}}$

$W SR_{0}$

$W SR_{8}$

Combinatorial Logic: Inverters

$dly = path\ delay\ from\ DFF\ to\ DFF$
Counter Arrays

- DUT contains two sets of the following:
  - 200 8-bit counters
  - 200 8-bit snapshot registers
- All counters and snapshot registers are connected to the same clock tree and RESET.
- The clock tree is fed by the CLK input from the LCDT.
- DUT CLK is connected to a DGBIO and a CLKBUF.
- The LCDT sends a clock and a reset to the DUT. The controls are set by the user.

Counts can still operate after most SEUs. However after an SEU occurs, the tester must recalculate a new expected value for the affected counter.

2 sets of counter arrays are tested simultaneously.
Test Facility Conditions: Texas A&M University Cyclotron Facility

- 25 MeV/amu tune.
- Flux: 1 x $10^4$ to 5 x $10^5$ particles/cm$^2$·s
- Fluence: All tests were run to 1 x $10^7$ particles/cm$^2$ or until destructive or functional events occurred.
- Test temperature: Room temperature

<table>
<thead>
<tr>
<th>Ion</th>
<th>Energy (MEV/Nucleon)</th>
<th>LET (MeV·cm$^2$/mg) 0°</th>
<th>LET (MeV·cm$^2$/mg) 60°</th>
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<tr>
<td>He</td>
<td>25</td>
<td>.07</td>
<td>.14</td>
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<tr>
<td>N</td>
<td>25</td>
<td>.9</td>
<td>.18</td>
</tr>
<tr>
<td>Ne</td>
<td>25</td>
<td>1.8</td>
<td>3.6</td>
</tr>
<tr>
<td>Ar</td>
<td>25</td>
<td>5.5</td>
<td>11.0</td>
</tr>
<tr>
<td>Kr</td>
<td>25</td>
<td>19.8</td>
<td>40.0</td>
</tr>
<tr>
<td>Xe**</td>
<td>25</td>
<td>38.9</td>
<td>78.8</td>
</tr>
</tbody>
</table>

**We were unable to obtain Xe during our testing**
Test Facility Conditions: Lawrence Berkeley National Laboratory Cyclotron Facility

- 16 MeV/amu tune.
- Flux: $1 \times 10^4$ to $5 \times 10^5$ particles/cm$^2 \cdot $s
- Fluence: All tests were run to $1 \times 10^7$ particles/cm$^2$ or until destructive or functional events occurred.
- Test temperature: Room temperature

<table>
<thead>
<tr>
<th>Ion</th>
<th>Energy (MEV/Nucleon)</th>
<th>LET (MeV*cm$^2$/mg) 0°</th>
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</thead>
<tbody>
<tr>
<td>N</td>
<td>16</td>
<td>1.16</td>
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<tr>
<td>Ne</td>
<td>16</td>
<td>2.39</td>
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<tr>
<td>Si</td>
<td>16</td>
<td>4.35</td>
</tr>
<tr>
<td>Ar</td>
<td>16</td>
<td>7.27</td>
</tr>
<tr>
<td>V</td>
<td>16</td>
<td>10.9</td>
</tr>
<tr>
<td>Cu</td>
<td>16</td>
<td>16.5</td>
</tr>
<tr>
<td>Kr</td>
<td>16</td>
<td>25</td>
</tr>
<tr>
<td>Xe</td>
<td>16</td>
<td>49.3</td>
</tr>
</tbody>
</table>
Heavy-Ion Configuration Re-programmability Results

- During this test campaign, tests were only performed up to an LET of 49.3 MeV cm$^2$/mg.
- Higher LETs will be used during future testing.
- No re-programmability failures were observed up to an LET of 49.3 MeV cm$^2$/mg when within particle dose limits. We did not try to reprogram while the beam was turned on.
Heavy-ion Global Route Results

• Global routes are the backbone of all designs. Hence, it is imperative to investigate global route SEU susceptibility.

• For NEPP DUT test structures, clock trees were connected to a variety of global clock tree sources:
  – Direct clock I/O
  – Internal Oscillator
  – Clock conditioning circuit (PLL)
  – TMR clock conditioning circuit (TMR PLL)

• Summary of global route results starting from best performance:
  – Direct clock I/O had the lowest SEU susceptibility (best performance.
  – Clock conditioning circuit had higher SEU susceptibility than direct clock I/O. However, performance can still be acceptable for critical missions.
  – TMR clock conditioning circuit (TMR PLL) did not appear to reduce susceptibility and might have higher susceptibility at higher frequencies.
  – Internal OSC is SEU soft and should not be used in critical circuits.
Rev C: WSRs with SET FILTER versus LET at 100MHz

Add combinatorial logic, increase cross section.

How and what you test make a big difference!

\[ \sigma_{SEU} (\text{cm}^2/\text{DFF}) \]

LET MeV*cm^2/mg

WSR16 Checkerboard
WSR8 Checkerboard
WSR4 Checkerboard
WSR0 Checkerboard
WSR16 All 1's
WSR8 All 1's
WSR4 All 1's
WSR0 All 1's
WSR16 All 0's
WSR8 All 0's
WSR4 All 0's
WSR0 All 0's
WSR and Counter Accelerated Radiation Test Data Observations

• WSR chains showed a variety of dependencies (all are as expected):
  – Increase clock frequency – increase failures.
  – Increase combinatorial logic – increase failures.
  – Increase data change rate – increase failures.
  – Use of flip-flop SET filter – decrease failures.
  – Use of flip-flop SET filter – decreases system operation speed.

• As LET increases, the effectiveness of the SET filter decreases. This is because generated SETs become wider (more energy) and have more power to defeat the SET filter.

• Results (SET filter on) are in-line with the Microsemi SEU radiation hardened predecessor – Microsemi RTAXs family.

• However, the Microsemi RTAXs family had slightly better SEU performance.
RTAX4000D and RTAX2000 WSRs at 80MHz with Checkerboard Pattern

RTAX4000D and RTAX2000 have better SEU performance than RTG4 (higher LET_{on-set}; and slightly lower σ_{SEUs}); but not by much.
Microsemi SRAM SEU Cross-Sections versus LET

**EDAC was only tested with μSRAM**

**μSRAM**

**Large SRAM Microsemi included**  
**SRAM bit interleaving.**  
**Makes a difference with EDAC.**

To be presented by Melanie Berg at the NASA Electronics Parts and Packaging (NEPP) Electronics Technology Workshop (ETW), Greenbelt, MD, June 26–29, 2017
Microsemi Math Block Test Structures

- 18x18 multiply accumulate math-blocks.
- Dual redundant chains with a compare.
- Coefficients are shared.

\[ P_n = P_{n-1} + \text{CARRYIN} + C + (A_0 \cdot B_0) \]
RTG4 Math-block (DSP) SEU Cross-Sections versus LET

As LET increases, the SET filter is not as effective. This is as expected.

As LET increases, the SET filter is not as effective. This is as expected.

18x18 multiply accumulate math-blocks

No errors observed DSP No Feedback SET filter
Deliverables: Microsemi RTG4 Test Report Submission and Data Summary

- Two versions of reports have been submitted.
- Third version will be completed by June 2017.
- As a summary:
  - RTG4 is not as SEU hardened as it’s predecessor (RTAXs). However, fairly close.
  - Exception: embedded SRAM with EDAC – is better in the RTG4.
  - Embedded TMR PLL does not operate as expected. No improvement in SEU susceptibility.
  - Internal Oscillator PLL is highly susceptible to SEUs.
  - Designs implemented in the RTG4 device do not operate as fast as they do when implemented in the RTG4’s predecessor (RTAXs). This is most likely due to the place and route software. However, this is unexpected.
  - TBD for NEPP to perform more testing. At this point, additional testing is assumed to be funded by partners or missions.
SRAM-based FPGA Mitigation Study using Xilinx Kintex-Ultrascale (XCKU040-1LFFVA1156I)
(1) Single event latch-up (SEL) and (2) Mitigation
Impact to Community
Kintex-UltraScale

$\sigma_{SEU}$: SEU Cross-section  $IP$: intellectual property

- Next generation of FPGA devices from the commercial Xilinx-7 series.
- I/O interfaces are significantly more robust
- There are no embedded mitigation. However, additional gate-count better allows the user to insert mitigation into the design.
- There is no embedded processor. However, the user can embed a soft-core or use the Zync-UltraScale (contains hard-IP processor cores).

$P(fs)_{system} = \mu P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$

$Design \sigma_{SEU}$  $Configuration \sigma_{SEU}$  $Functional logic \sigma_{SEU}$  $SEFI \sigma_{SEU}$

**NEPP performs an independent study to determine the level of SEU susceptibility for the various FPGA components.**
### Xilinx Kintex-Ultrascale

- **New Entry into the Aerospace Market with COTS Expectation … 20 nm planar process (TSMC).**

**Data Transfer Is Key for Our New System Applications:** *UltraScale Transceivers*

<table>
<thead>
<tr>
<th></th>
<th>Kintex-Ultrascale</th>
<th>Virtex UltraScale</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Type</strong></td>
<td>GTH</td>
<td>GTH</td>
</tr>
<tr>
<td><strong>Quantity</strong></td>
<td>16-64</td>
<td>0-32</td>
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<tr>
<td><strong>Maximum Data Rate</strong></td>
<td>16.3Gb/s</td>
<td>16.3Gb/s</td>
</tr>
<tr>
<td><strong>Minimum Data Rate</strong></td>
<td>0.5Gb/s</td>
<td>0.5Gb/s</td>
</tr>
<tr>
<td><strong>Key Applications</strong></td>
<td>Backplane PCIe Gen4 HMC</td>
<td>Backplane PCIe Gen4 HMC</td>
</tr>
</tbody>
</table>
Xilinx Kintex-UltraScale Study Objectives

- This is an independent investigation that evaluates the single event destructive and transient susceptibility of the Xilinx Kintex-UltraScale device.
- Design/Device susceptibility is determined by monitoring the DUT for Single Event Transient (SET) and Single Event Upset (SEU) induced faults by exposing the DUT to a heavy ion beam.
- Potential Single Event Latch-up (SEL) is checked throughout heavy-ion testing by monitoring device current.
- This device does not have embedded mitigation. Hence, user implemented mitigation is investigated using Synopsys mitigation tools.
- FPGA part# XCKU040-1LFFVA1156I.
- Collaboration: Xilinx and Synopsys.

*Beam time was limited: SEL, configuration, and Mitigation.*
# TMR Descriptions

**DFF**: Edge triggered flip-flop;  
**CL**: Combinatorial Logic

<table>
<thead>
<tr>
<th>TMR Nomenclature</th>
<th>Description</th>
<th>TMR Acronym</th>
</tr>
</thead>
<tbody>
<tr>
<td>Block TMR</td>
<td>Entire design is triplicated. Voters are placed at the outputs.</td>
<td>BTMR</td>
</tr>
<tr>
<td>Local TMR</td>
<td>Only the DFFs are triplicated. Voters are placed after the DFFs.</td>
<td>LTMR</td>
</tr>
<tr>
<td>Distributed TMR</td>
<td>DFFs and CL-data-paths are triplicated. Similar to a design being triplicated but voters are placed after the DFFs.</td>
<td>DTMR</td>
</tr>
<tr>
<td>Global TMR</td>
<td>DFFs, CL-data-paths and global routes are triplicated. Voters are placed after the DFFs.</td>
<td>GTMR or XTMR</td>
</tr>
</tbody>
</table>

Note: It has been suggested to separate (partition) TMR domains in SRAM based designs so that there are no overlapped shared resources. Shared resources become single points of failure.
DTMR Partitioning

SEUs that occur in one TMR domain are expected to be mitigated.
# Kintex-Ultrascale Designs Tested

<table>
<thead>
<tr>
<th>Test Structure</th>
<th>Frequency Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Counter Array No TMR</td>
<td>50MHz</td>
</tr>
<tr>
<td>Counter Array DTMR with partitioning</td>
<td>50MHz</td>
</tr>
<tr>
<td>Counter Array DTMR no partitioning</td>
<td>50MHz</td>
</tr>
<tr>
<td>Counter Array BTMR with partition</td>
<td>50MHz</td>
</tr>
<tr>
<td>Counter Array LTMR with partition</td>
<td>50MHz</td>
</tr>
</tbody>
</table>

**NEPP has the only current heavy-ion data for the Synopsys mitigation tool.**
Test Facility Conditions

• Flux: $1 \times 10^4$ to $5 \times 10^5$ particles/cm$^2$·s
• Fluence: All tests were run to $1 \times 10^7$ particles/cm$^2$ or until destructive or functional events occurred.
• Test temperature: Room temperature

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We were unable to obtain Xe during our testing
Kintex-UltraScale DUT And Tester
Xilinx Scaling Family Trends for Configuration Bits in Heavy Ions

David Lee et. al. “Single-Event Characterization of the 20 nm Xilinx Kintex UltraScale Field-Programmable Gate Array under Heavy Ion Irradiation”

https://www.osti.gov/scitech/servlets/purl/1263983

Daily upsets in configuration in LEO and GEO are expected.
History of Xilinx and Single Event Latchup (SEL) or Latchup-Like Events: Virtex 2 through UltraScale Series

- Xilinx Virtex 2: Latchup-like events have been observed in flight. Most likely due to embedded half-latches in the device.
- Xilinx Virtex 5: Half-latches were removed. No latchup-like events observed during SEE testing or in flight.
- Xilinx 7-series: Is it SEL or latchup-like? Observed only on 7-series devices that contained 3.3V I/O. Devices that do not contain such I/O have no latchup-like events.
- Xilinx UltraScale series no latchup-like event observed.
Kintex-UltraScale Data drops off quicker than radiation hardened Xilinx Virtex (V5QV).

More SEU testing should be performed for more detailed comparisons.
Comparison of V5QV and Kintex UltraScale with Mitigation

**V5QV Counters**

- V5QV Counter Filter Off
- V5QV Counter Filter ON

**Kintex UltraScale DTMR Counters**

- Kintex UltraScale Partition
- Kintex UltraScale No Partition

**Synopsys results are looking good.**
Summary of Mitigation Application to Kintex-UltraScale during SEU-Heavy-Ion Testing

SEFI: single event functional interrupt

• Mitigation study proves DTMR is the strongest mitigation scheme implemented in an SRAM-based FPGA.
  – However, for flushable designs BTMR might be acceptable.
  – LTMR is not acceptable in SRAM-based FPGAs for any design.
  – Partitioning may not be necessary.

• Although GTMR has been implemented in V5 families and earlier Xilinx device families, NEPP has suggested to avoid GTMR because clock skew is difficult to control.
  – In 2015-2016, via heavy-ion SEU testing, It has been observed in the Xilinx 7-series, that race conditions due to clock skew are unavoidable.
  – This is due to the speed of combinatorial logic and route delays in the 7-series versus earlier Xilinx FPGA device families.

• Synopsis tool has improved for simple designs. They are still working on IP core instantiations and other challenges.

• Mitigation and IP cores are still a major concern!!!!!!!!!!!!!!!
Deliverables: Xilinx Kintex-UltraScale Test Report Submission and Data Summary Test Report

• The full Kintex-UltraScale SEU dataset is still currently being analyzed and will be available by June 2017.

• As a summary:
  – NEPP has provided insight into Xilinx potential latch-up-like events.
  – Through previous testing and design experience, NEPP has provided Synopsys with information for sufficient mitigation strategies per FPGA.
  – TBD for NEPP to perform more testing. At this point, additional testing is assumed to be funded by partners or missions.
Xilinx Zynq UltraScale+

• New Entry into the Aerospace Market with COTS Expectation.
  – 16nm FinFet vertical process (TSMC).
  – Depending on mission requirements, additional mitigation may be required.

• Zync UltraScale+ Includes:
  – Dual and quad core variants of the ARM Cortex-A53 (APU).
  – Dual-core ARM Cortex-R5 (RPU).
  – Dedicated ARM graphics processing unit (GPU).

SRAM based Configuration. No radiation hardening is applied to flip-flops. However, manufacturer hopes FinFET technology will reduce SEU susceptibility.
### Xilinx Kintex-Ultrascale+ Transceivers

#### Data Transfer Is Key for Our New System Applications: UltraScale+ Transceivers

<table>
<thead>
<tr>
<th></th>
<th><strong>Kintex-Ultrascale+</strong></th>
<th><strong>MPSoC UltraScale+</strong></th>
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</thead>
<tbody>
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<td>GTY</td>
</tr>
<tr>
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<td></td>
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<td>0-28</td>
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<tr>
<td><strong>Maximum Data Rate</strong></td>
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<tr>
<td></td>
<td>6.0Gb/s</td>
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<td></td>
<td>32.75Gb/s</td>
<td>32.75Gb/s</td>
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<tr>
<td><strong>Minimum Data Rate</strong></td>
<td>0.5Gb/s</td>
<td>0.5Gb/s</td>
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<tr>
<td></td>
<td>1.25Gb/s</td>
<td>0.5Gb/s</td>
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<td>0.5Gb/s</td>
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<td><strong>Key Applications</strong></td>
<td>Backplane PCIe Gen4 HMC</td>
<td>100G+Optics Chip-to-Chip 25G+ Backplane HMC</td>
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<td>PCIe Gen2 USB Ethernet</td>
<td>PCIe Gen4 HMC</td>
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<td>Backplane PCIe Gen4 HMC</td>
<td>Backplane PCIe Gen4 HMC</td>
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<td>100G+Optics Chip-to-Chip 25G+ Backplane HMC</td>
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Xilinx UltraScale+ Schedule

• We plan to test two platforms:
  – MPSoC evaluation board.
  – Custom Kintex-Ultrascale+ daughter card. Designed by NEPP.
• We currently have one evaluation board. MPSoC evaluation boards (ready for testing) will be in hand in June 2017.
• Proton testing using the MPSoC evaluation board is planned for August 2017 timeframe.
• Custom board is planned to be completed October 2017.
• Heavy ion testing will occur FY17 and FY18.
• Current Partners:
  – NASA Goddard Science Data Processing Branch,
  – JPL, and
  – Sandia National Laboratory
  – Xilinx
  – We are looking for additional collaboration.
Development of New Methodology for Characterizing SEU System Response (1)

- This study transforms proven classical reliability models into the SEU particle fluence domain. The intent is to better characterize SEU responses for complex systems.
- Will be discussed in further detail in another ETW presentation.
- Deliverables:
  - Development of analysis (ongoing).
Development of New Methodology for Characterizing SEU System Response (2)

- The proposed method does not rely on data-fitting and hence removes a significant source of error.
- The proposed method provides information for highly SEU-susceptible scenarios; hence enabling a better choice of mitigation strategy.
- This methodology expresses SEU behavior and response in terms that missions understand via classical reliability metrics.

Presentations:
- Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2017 in Reno, NV.
- Submission to IEEE Radiation and its Effects on Components and Systems (RADECS) 2017. Conference will be held in Geneva, SUI.
FPGA Security and Trust

- **Goal:** Support the U.S. government concerns regarding security and trust in FPGAs.
- **Conference participation:**
  - Xilinx Security Working Group (XSWG) 2016 in Longmont, CO.
  - Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2017 in Reno, NV.
  - Hardened Electronics and Radiation Technology (HEART) 2017 in Denver, CO.
  - Hardware-Oriented Security and Trust (HOST) 2017, McLean, VA.
  - Joint Federated Assurance Center (JFAC) FPGA working group: Trusted Microelectronics Special Topic: Field Programmable Gate Array Assurance Workshop, McLean, VA.
- **Collaboration with Aerospace Corporation, JFAC, and other agencies.**
  - Meetings, consultations, and presentations.