Silicon Power MOSFETs

Jean-Marie Lauenstein, Megan Casey, Mike Campola, Ray Ladbury, and Ken LaBel - NASA/GSFC
Ted Wilcox, Anthony Phan, Hak Kim, and Alyson Topper, AS&D, Inc.

Acknowledgment:
This work was sponsored by:
NASA Office of Safety & Mission Assurance
in collaboration with:
NASA Engineering and Safety Center
# Abbreviations & Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>BV&lt;sub&gt;DSS&lt;/sub&gt;</td>
<td>Drain-Source Breakdown Voltage</td>
</tr>
<tr>
<td>COTS</td>
<td>Commercial Off The Shelf</td>
</tr>
<tr>
<td>EEE</td>
<td>Electrical, Electronic, and Electromechanical</td>
</tr>
<tr>
<td>ETW</td>
<td>Electronics Technology Workshop</td>
</tr>
<tr>
<td>FY</td>
<td>Fiscal Year</td>
</tr>
<tr>
<td>GCR</td>
<td>Galactic Cosmic Ray</td>
</tr>
<tr>
<td>I&lt;sub&gt;D&lt;/sub&gt;</td>
<td>Drain Current</td>
</tr>
<tr>
<td>I&lt;sub&gt;DSS&lt;/sub&gt;</td>
<td>Drain-Source Leakage Current</td>
</tr>
<tr>
<td>I&lt;sub&gt;G&lt;/sub&gt;</td>
<td>Gate Current</td>
</tr>
<tr>
<td>LBNL</td>
<td>Lawrence Berkeley National Laboratory cyclotron facility</td>
</tr>
<tr>
<td>LET</td>
<td>Linear Energy Transfer</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>NEPP</td>
<td>NASA Electronic Parts and Packaging</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>NESC</td>
<td>NASA Engineering &amp; Safety Center</td>
</tr>
<tr>
<td>PIGS</td>
<td>Post Irradiation Gate Stress</td>
</tr>
<tr>
<td>RHA</td>
<td>Radiation Hardness Assurance</td>
</tr>
<tr>
<td>RTN</td>
<td>Random Telegraph Noise</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>SJ</td>
<td>Superjunction</td>
</tr>
<tr>
<td>SOA</td>
<td>State Of the Art</td>
</tr>
<tr>
<td>SWAP</td>
<td>Size, Weight, And Power</td>
</tr>
<tr>
<td>TAMU</td>
<td>Texas A&amp;M University cyclotron facility</td>
</tr>
<tr>
<td>TID</td>
<td>Total Ionizing Dose</td>
</tr>
<tr>
<td>VDMOS</td>
<td>Vertical Double-diffused MOSFET</td>
</tr>
<tr>
<td>V&lt;sub&gt;DS&lt;/sub&gt;</td>
<td>Drain-Source Voltage</td>
</tr>
<tr>
<td>V&lt;sub&gt;GS&lt;/sub&gt;</td>
<td>Gate-Source Voltage</td>
</tr>
<tr>
<td>V&lt;sub&gt;TH&lt;/sub&gt;</td>
<td>Gate Threshold Voltage</td>
</tr>
</tbody>
</table>
Outline

• Power MOSFET Task & Technology Focus
• Task Roadmap & Partners
• Recent Results
• Summary & Comments

_Trench-style MOSFETs offer application-targeted performance enhancements but are more vulnerable to ion-induced TID degradation_

Lauenstein, IEEE REDW 2013
Silicon Power MOSFET Technology

Planar Gate VDMOS
- Dominates rad-hardened offerings
- Prior NEPP efforts helped to expand market

Trench Gate VDMOS
- Dominates COTS lower-V applications
- Only 1 rad-hardened offering

Trench SJ VDMOS
- Emerging technology

Superjunction (SJ) VDMOS
- COTS competes with IGBTs
- Near-term availability of rad-hardened options for 100V-650V (100V – 250V out now…for a $$)

Drawings from:
Lauenstein, IEEE REDW 2013
Silicon Power MOSFET Technology

- NEPP task focuses on RHA of state-of-the-art Si power MOSFETs offering competitive edge over older planar gate VDMOS

- Trench Gate VDMOS
  - Dominates COTS lower-V applications
  - Only 1 rad-hardened offering

- Trench SJ VDMOS
  - Emerging technology

- Superjunction (SJ) VDMOS
  - COTS competes with IGBTs
  - Near-term availability of rad-hardened options for 100V-650V applications
Motivational Factors

Game-changing NASA approaches are demanding higher-performance power electronics

- SWAP benefits for existing technologies

Conclusions: We must understand risks of COTS/Auto options;
We must foster industry partnerships to develop rad-hardened options when feasible
NEPP Collaborations

- Informal relationships include assisting end-users:
  - Understanding radiation effects and sharing test data on power MOSFETs to aid parts selection
  - Best practices, “rules of thumb” for application conditions
Silicon Power MOSFET Roadmap

Rad Hardened
- STMicro superjunction
- Infineon superjunction 100 V, higher-V targeted
- Fuji JAXA-R VDMOS high voltage
- Microsemi i2MOS
- Infineon (IR) R8 trench

COTS/Alternative Grade
- Vishay Trench
- On Semiconductor Trench
- NKP Trench

Radiation Testing (track status)

FY15 FY16 FY17 FY18

To be presented by Jean-Marie Lauenstein at the NASA Electronics Parts and Packaging (NEPP) Electronics Technology Workshop (ETW), Greenbelt, MD, June 26-29, 2017.
Silicon Trench Power MOSFET Catastrophic Failure Modes

- **COTS/Automotive:**
  - Collaborative effort with NESC
  - *Part-part variability requires larger test sample sizes, possibly more derating*
  - N-type – SEB
    - *Onset LET varies within manufacturer*
      - Cannot generalize test results
    - Even for LETs below GCR “iron knee”, must use these 60 V parts at < 50 %
  - P-type – SEGR
    - Often safe at higher % of rated voltage

Comparison of n-type 60V trench MOSFET SEB thresholds

Trench MOSFETs on test board at Lawrence Berkeley National Laboratory accelerator facility

To be presented by Jean-Marie Lauenstein at the NASA Electronics Parts and Packaging (NEPP) Electronics Technology Workshop (ETW), Greenbelt, MD, June 26-29, 2017.
P-Type Trench Power MOSFET Test Results

Vishay SQJ431EP Automotive: -200V, 12A, 213 mΩ

SEGR with 886 MeV krypton (LET = 31 MeV·cm²/mg) at 75% of rated voltage

- “×” in left plot marks failure after first beam run at -150 V: threshold thus not found.
- 2 samples failed on PIGS; 1 during run (gate-to-drain) (right plot)
P-Type Trench Power MOSFET Test Results (cont’d)

On Semiconductor NVTFS5116PL Automotive: -60V, 14A, 52 mΩ

- SEGR with 886 MeV krypton (LET = 31 MeV·cm²/mg) at 83% of rated voltage
  - All 3 samples failed during run (ex/ right plot)
  - Part-to-part variability: may require additional derating over standard 0.75 factor
    - Ex/ 0.75*(-50 V) = -37.5 V but 99/90 one-sided tolerance (KTL) yields -30 V

To be presented by Jean-Marie Lauenstein at the NASA Electronics Parts and Packaging (NEPP) Electronics Technology Workshop (ETW), Greenbelt, MD, June 26-29, 2017.
P-Type Trench Power MOSFET Test Results (cont’d)

Nexperia BSS84AKV Automotive: -50V, 170mA, 7.5 Ω

- SEGR with 886 MeV krypton (LET = 31 MeV·cm²/mg) at 88% of rated voltage
  - All 3 samples failed during run (ex/ right plot)
  - Part-to-part variability: may require additional derating over standard 0.75 factor

- Cannot rule out bimodal distribution

SEGR Response Curve

To be presented by Jean-Marie Lauenstein at the NASA Electronics Parts and Packaging (NEPP) Electronics Technology Workshop (ETW), Greenbelt, MD, June 26-29, 2017.
N-Type Trench Power MOSFET Test Results

Vishay SQS460EN
Automotive: 60V, 8A, 36 mΩ

Vishay Si7414DN
COTS: 60V, 8.7A, 25 mΩ

SEB Response Curve

- SEB with ions below the GCR “iron knee”, at 50% of rated voltage
  - Possible risk of SEB in proton environment
  - Part-to-part variability/bimodality continues to be a concern
N-Type Trench Power MOSFET Test Results: 200 MeV Protons

Vishay Si7414DN COTS: 60V, 8.7A, 25 mΩ

Strip Tape During Run:
Charge Collection Only

Strip Tape During Run:
Current Spikes

- Onset $V_{DS}$ for current spikes from 200-MeV protons is similar to that of SEB from heavy ions
  - Lack of stiffening capacitor may have allowed $V_{DS}$ quenching
N-Type Trench Power MOSFET
Test Results: 200 MeV Protons (cont’d)

Vishay Si7414DN COTS: 60V, 8.7A, 25 mΩ

Proton Test Setup

MIL-STD Test Circuit

- Frequency of current spikes, but not magnitude, increases at higher $V_{DS}$
  - Additional tests needed to reveal whether spikes are protective-mode SEB events

Strip Tape During Run:
Increased Current Spike Frequency
Silicon Trench Power MOSFET Degradation from Heavy Ions

- Non-hardened n-type susceptible to localized dosing degradation
  - Ion strike through gate oxide locally shifts the flatband voltage, forming a transistor region with lower gate threshold voltage
  - Well-understood phenomenon affecting only n-type transistors
    - Gate threshold shift in p-type swamped by overall lower threshold voltage

Strikes through gate oxide along channel length form regions of lower $V_{\text{TH}}$

Greater effect on $V_{\text{TH}}$ from heavy ions vs. protons

To be presented by Jean-Marie Lauenstein at the NASA Electronics Parts and Packaging (NEPP) Electronics Technology Workshop (ETW), Greenbelt, MD, June 26-29, 2017.
Silicon Trench Power MOSFET Degradation from Heavy Ions (cont’d)

• Magnitude of effect is primarily voltage-dependent
  – On orbit, unbiased spares are still vulnerable

To be presented by Jean-Marie Lauenstein at the NASA Electronics Parts and Packaging (NEPP) Electronics Technology Workshop (ETW), Greenbelt, MD, June 26-29, 2017.
Hardened Trench MOSFET Test Results

Infineon (International Rectifier) IRHLF87Y20
R8 rad-hardened: 20V, 12A, 32 mΩ

- First (and only) rad-hardened trench MOSFET
  - Verified manufacturer SOA
  - 3 different failure signatures occurred outside SOA
    - Greater complexity than planar MOSFETs

SEE Response Curve

SEB (note RTN-like behavior)  SEGR  SEB with partial recovery

1039 MeV Ag  V_{ds}=20 V  V_{ds}=0 V

To be presented by Jean-Marie Lauenstein at the NASA Electronics Parts and Packaging (NEPP) Electronics Technology Workshop (ETW), Greenbelt, MD, June 26-29, 2017.
Summary and Comments

• Commercial and alternative-grade MOSFET usage will continue
  – Driven by higher risk-tolerant missions & commercial space
  – RHA challenge in light of limited funding:
    • Understand general radiation effects
    • Become wiser at identifying “must test” candidates
      – By application & environment
      – By component itself (voltage rating, type, manufacturer, etc.)

• Higher-performing radiation-hardened options are on the horizon

• Partnering is the key to incentivize manufacturers of rad-hardened parts and to share COTs data
  – Government
  – Industry
  – Academia