SPICE Modeling of Body Bias Effect in 4H-SiC Integrated Circuit Resistors

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As progressively complex 4H-SiC junction field effect transistor (JFET) integrated circuits (ICs) have reproducibly demonstrated operation for thousands of hours at $T > 460 \, ^\circ\mathrm{C}$, interest in usefully fielding these uniquely durable chips in harsh environment missions has grown [1-3]. Regardless of the circuit complexity, these ICs are made from on-chip interconnection of just two fundamental device types: (1) n-channel 4H-SiC JFETs and (2) n-channel 4H-SiC resistors. In order to maximize availability and ease of use for prospective circuit designers, JFET and resistor models compatible with baseline-version SPICE circuit modeling software have been developed [4]. However, the baseline-version SPICE semiconductor resistor R model, which is the basis for the 4H-SiC resistor model approximation reported in [4], makes no provision for substrate body bias effect. This report examines body effect measured in 4H-SiC IC resistors and describes the use of NMOS-based models for more accurate simulation of DC resistor behavior in SPICE.

Figure 1 schematically reviews the cross-section of 4H-SiC IC resistors illustrating applied anode $V_A$ and substrate $V_S$ bias. Figure 2 shows measured (dashed lines) current vs. voltage (I-V) characteristics at 27 °C and 500 °C for a 480 $\mu\mathrm{m} \times 6 \, \mu\mathrm{m}$ resistor that exemplifies the major observed IC resistor body bias behaviors compared to the linear (i.e., without body effect) SPICE resistor model simulations (solid lines). The measured (dashed) I-V characteristics bend down consistent with the fact that bias across the substrate-channel pn junction somewhat depletes the conductive n-channel near the anode end of the resistor where positive I-V measurement bias is applied. As seen in Fig. 2, the significant discrepancy between measured resistor I-V data and linear SPICE semiconductor resistor model grows larger with increasing magnitude of $V_A$ and $V_S$. Extraction of differential resistance $R_{diff} = dV_A/dI_A$ (Fig. 2, light blue) quantifies change in device resistance as the anode measurement voltage $V_A$ is swept.

As the n-channel SiC IC resistors reside on top of p-epilayer/substrate (Fig. 1), the resistors are structurally equivalent to long-channel buried-gate JFETs wherein the p-epilayer/substrate serves as the gate terminal. The magnitude of negative $V_S$ required to completely deplete the n-channel is large since $N_{\text{DC}} \gg N_{\text{AC}}$ in Fig. 1. Therefore, the “JFET” operates in the linear region, and the SPICE modeling parameters can be extracted from measured I-V data [5]. Similar to prior SiC JFET modeling work [4], the baseline SPICE NMOS model is used for modeling, wherein substrate bias $V_S$ is applied to the gate terminal of the NMOS device instance in SPICE.

Figure 3 compares SPICE-simulated resistor I-Vs with measured resistor I-Vs for $V_S = 0 \, \text{V}$ and $V_S = -25 \, \text{V}$ at 27 °C and 500 °C. The SPICE NMOS modeled I-Vs (dashed green) provide far better match to measured (dashed light blue) resistor I-V data compared to the linear SPICE R model without body effect (solid blue), especially for $V_S \approx -25 \, \text{V}$ substrate bias conditions employed in 1000+ hour 500 °C integrated circuit demonstrations [1,2]. Text input listings for the Fig. 3 I-V simulations are given below each plot to illustrate correct SPICE code for modeling IC resistors with body effect as NMOS devices.

Fig. 1. 4H-SiC IC resistor cross-section with depletion regions affecting n-channel resistance.

Fig. 2. Comparisons of DC measured 80-square resistor I-V characteristics (dashed lines) with linear resistor model simulations (solid lines) at $V_S$ of 0 V, -15 V, and -25V at (a) 27 °C and (b) 500 °C.

Fig. 3. I-V comparison of linear R SPICE resistor model (solid dark blue) and NMOS SPICE body-effect resistor model (dashed green) with measured data (dashed light blue) for a 480μm x 6μm resistor at (a) 27°C and (b) 500 °C. The SPICE codes for the NMOS simulations are also shown.