Prolonged 500 °C Operation of 100+ Transistor Silicon Carbide Integrated Circuits

David J. Spry\textsuperscript{1}, Philip G. Neudeck\textsuperscript{1}, Dorothy Lukco\textsuperscript{2}, Liangyu Chen\textsuperscript{3}, Michael J. Krasowski\textsuperscript{1}, Norman F. Prokop\textsuperscript{1}, Carl W. Chang\textsuperscript{2}, Glenn M. Beheim\textsuperscript{1}

\textsuperscript{1}NASA Glenn Research Center
\textsuperscript{2}Vantage Partners LLC
\textsuperscript{3}Ohio Aerospace Institute
SiC Electronics Benefits to NASA Missions

Intelligent Propulsion Systems

Venus Exploration

LLISSE = Long-Life In-Situ Solar System Explorer

Hybrid Electric & Turbo Electric Aircraft

NASA GRC’s internal research effort has been focused on durable/stable integrated circuit operation at 500 °C for > 1000 hrs.

9.4 Mpa = 92.7X Earth pressure + 460 °C + chemical composition found at the surface of Venus (CO₂, N₂, SO₂, H₂O, CO, OCS, HCl, HF, and H₂S)

Recent Advances


NASA SiC JFET IC operation at T > 900 °C

NASA SiC JFET IC operated directly immersed in Venus surface conditions (no package) for 3 weeks (did not fail)
N-channel JFET design\textsuperscript{1,2} “Version 10.1”

- Normally-on 4H-SiC JFET (fabricated at NASA Glenn)
- Resistors made with same epi as channel → matched T dependence
- Negative threshold voltage $V_T$ → negative signal voltages (0 to -10V)
- 0 V = Binary 1 (high) \hspace{1cm} -10 V = Binary 0 (low)

\textsuperscript{1} M. J. Krasowski, US Patent 7,688,117 (2010).
JFET IC Wafer 10.1 vs past work\(^{1,2}\)

- **Aluminum** Field Stop Implant to impede parasitic field MOSFETs.
- Heavily-implanted SiC contact regions were formed using **phosphorus** implant profile with slightly lower energy & dose.
- Contact was made using 50 nm sputtered **titanium** layer.

---


High-T packaging$^{1,2}$ (32 pins)

- Package durability and leakage characterized.

4X4 Random Access Memory (RAM) Demonstration Chip

- 3mm x 3mm 4H-SiC JFET chip shown prior to packaging.
- 195 JFETs.
- 6-Transistor static RAM cell approach.
- Includes address decoders, read/write bitline drive with sense amplifiers, output buffers.
\[ \div2/\div4 \text{ Clock Demonstration Chip} \]

- 3mm x 3mm 4H-SiC JFET chip prior to packaging.
- 175 JFETs
- 21-Stage ring oscillator provides base frequency clock signal
- SELECT data line:
  - High (0 V) \( \rightarrow \div4 \) output
  - Low (-10 V) \( \rightarrow \div2 \) output
- Includes two D-type flip flops governed by select logic
  - 3rd flip flop is inactive due to layout error.
- Optional modulation of high-f ring oscillator signal
Wafer 10.1 IC Functional Yield at 25 °C

Table I. 25 °C Probe Test Yield for 100+ JFET SiC ICs

<table>
<thead>
<tr>
<th>Demonstration IC</th>
<th>IC JFET Count</th>
<th># Good/# Tested</th>
<th>% Yield r ≤ 25 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-bit RAM</td>
<td>195</td>
<td>19/27</td>
<td>70%</td>
</tr>
<tr>
<td>÷ 2/÷ 4 Clock</td>
<td>175</td>
<td>19/26</td>
<td>73%</td>
</tr>
</tbody>
</table>

• Probe-test measurements at 25 °C prior to wafer dicing and circuit packaging.

• JFET threshold voltage $V_T$ on depends on distance from the center of the wafer $r$, due to as-purchased wafer epilayer variation (see Ref. 1).

• Table I is for $r < 25$mm (on 38 mm radius wafer), the wafer region where $V_T$ falls within circuit design specifications of $|V_T| < 10$ V.

## Wafer 10.1 500 °C Packaged IC Tests

### Table II. Summary of 500 °C Packaged IC Tests

<table>
<thead>
<tr>
<th>Packaged IC Sample</th>
<th>500 °C Test Hours</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-bit RAM #1</td>
<td>1525 h</td>
<td>Suspended</td>
</tr>
<tr>
<td>16-bit RAM #2</td>
<td>5040 h</td>
<td>Running</td>
</tr>
<tr>
<td>÷2/÷4 Clock #1</td>
<td>470 h</td>
<td>Failed</td>
</tr>
<tr>
<td>÷2/÷4 Clock #2</td>
<td>5200 h</td>
<td>Running</td>
</tr>
<tr>
<td>÷2/÷4 Clock #3A</td>
<td>4377 h</td>
<td>Running</td>
</tr>
<tr>
<td>÷2/÷4 Clock #3B</td>
<td>4377 h</td>
<td>Running</td>
</tr>
<tr>
<td>÷2/÷4 Clock #3C</td>
<td>2090 h</td>
<td>Failed</td>
</tr>
</tbody>
</table>

RAM#1 was tested as 12-bit due to damage/failure of one row/word line during packaging.
Clock chips 3A, 3B, 3C reside in same package.
• Measured 16-bit RAM waveforms showing read and write functionality of all bits at 5040 hours of a 500 °C oven test.

Prolonged 500 °C Operation of 100+ Transistor Silicon Carbide Integrated Circuits
• Measured waveforms showing operation of \( \div 2 / \div 4 \) clock IC at 5200 hours of 500 °C oven testing.
Time evolution of ÷2/÷4 clock IC output voltages and frequency for 5 packaged chips subjected to prolonged 500 °C oven testing.

After initial burn-in, output characteristics change < 10%

3 of 5 chips remain functioning under 500 °C test.
(a) Crack typical of prolonged $T \geq 500$ °C testing in air (727 °C for this sample)

- In Earth environment, the crack allows the top surface of the TaSi$_2$ film to oxidize which exacerbates failure.

(b) Crack in IC sample tested in Venus surface condition.

- In Venus environment, the crack reaches the top of the TaSi$_2$ but does not propagate through the TaSi$_2$ and there is no observable evidence of TaSi$_2$ film oxidation.
Other samples exposed to Venus

- Platinum forms Platinum Sulfide.
  - 200nm thick films completely converted.
- Many morphologies found dependent on surrounding materials.
- Transition metals react to form sulfides.
- Trace amounts of HCl at 0.5 ppm and HF at 2.5 ppb that were found as reacted products in some samples.
- Temperature and/or pressure without including the complete chemistry is not a sufficient means of screening electronics for long-term operation in the Venusian surface environment.
- SiC, SiO\textsubscript{2}, \textit{Al}_2\textit{O}_3 remain stable.
Summary

• The complexity of 4H-SiC JFET IC’s proven durable for 1000’s of hours at 500 °C has been substantially increased from 24 transistors to 175+ transistors.

• Testing in high-fidelity reproduction of the Venus surface environment is necessary to continue electronics development and qualification testing building towards long-term Venus surface missions.
Acknowledgements

Funded by NASA Transformative Aeronautics Concepts Program

HX5 Sierra
• Kelley Moses
• Jose Gonzalez
• Michelle Mardenovich
• Ariana Miller

NASA Glenn Research Center
• Gary Hunter
• Robert Buttler
• Roger Meredith

Case Western Reserve University
• Amir Avishai
STARC-ABL: Single-aisle Turboelectric AiRCraft with Aft Boundary Layer propulsion
Typical Crack Propagation in Earth Air

- This sample was at 727 °C sample and a old (Version 9.2) design. Same kind of behavior when seen on some 500 °C samples.
- Cracks related to dicing, handling, design rules, and bonding.
- Various degrees of oxidation and peeling seen.
- Oxidation of TaSi2 surface can be many 10s of microns wide.
Crack at Venus Surface Conditions

• Only one crack seen on entire sample exposed to Venus.
• Found via optical microscope and then examined on SEM. Hard to find with FESEM.
• Very small (~ 75 nm) when viewed from the top.