Incorporating Probability Models of Complex Test Structures to Perform Technology Independent FPGA Single Event Upset Analysis

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Abstract—We present SEU test and analysis of the Microsemi ProASIC3 FPGA. SEU Probability models are incorporated for device evaluation. Included is a comparison to the RTAXS FPGA illustrating the effectiveness of the overall testing methodology.

Index Terms—FPGA, ProASIC3 versus RTAXS, SEU, Test and Analysis

I. INTRODUCTION

A n effective method for modeling Single Event Upset (SEU) probabilities \( P(\text{error}) \) in Field Programmable Gate Array (FPGA) devices has been presented[1][2]. It is a top-down modeling approach. The top-level of the FPGA \( P(\text{error}) \) model was shown to have three major components (1):

- Configuration SEU cross section \( P(\text{configuration}) \)
- Data path or functional logic SEU cross section \( P(\text{FunctionalLogic}) \)
- Single Event Functional Logic SEU cross section \( P(\text{SEFI}) \)

\[
P(\text{error}) \propto P(\text{configuration}) + P(\text{FunctionalLogic}) + P(\text{SEFI})
\]

The SEU Probability model is used by NASA Goddard Radiation Effects and Analysis Group (REAG) as a Single Event Effects (SEE) data analysis tool. Upsets that occur during radiation testing are differentiated and are categorized in order to enhance device evaluation. The model is a reflection of the SEU cross section \( \sigma_{\text{SEU}} \) for a synchronous digital system. Operational frequency \( (f) \) is understood to be the inverse of clock period \( (\tau_{\text{clk}}) \) as in (2).

\[
\tau_{\text{clk}} = \frac{1}{f}
\]

The importance of this subject matter is to present Microsemi ProASIC3 FPGA SEU behavior under a variety of conditions while illustrating how the REAG SEU model facilitates a detailed analysis that spans across FPGA device technologies. Microsemi RTAXS data[2] will be used as a comparison.

II. \( P(\text{error}) \) MODEL COMPONENTS

Before radiation testing is performed, models of expected SEU probabilities based on mitigation and device logic structure are constructed. The models are used as reference points during radiation testing. During the analysis phase, the models are refined to reflect SEU results from radiation testing. The following is a more detailed discussion of each element in (1).

A. FPGA Configuration and \( P(\text{configuration}) \)

Configuration is a separate technology than the functional logic. Accordingly, it has its own categorization of upsets. It has been shown through Configuration SEE radiation testing of Antifuse[1][4] and Flash technologies[3][4] that \( P(\text{configuration}) \) is essentially zero as in (3).

\[
P(\text{configuration}) \rightarrow 0;
\]

The RTAXS has an antifuse configuration [7] while the ProASIC3 has a flash configuration [8]. Because \( P(\text{configuration}) \) is essentially zero for these devices, the following discussion focuses on \( P(\text{error})_{\text{FunctionalLogic}} \) and \( P(\text{SEFI}) \).

B. Functional Logic Data Path Upsets and \( P(\text{FunctionalLogic}) \)

The functional logic data path is comprised of: Combinatorial Logic, Flip-Flops (DFFs), and Routes. Table 1 illustrates upset types that can potentially occur in a FPGA data path. In a synchronous design, every DFF is connected to a global clock signal. Because a DFF is master-slave edge
flip-flop its internal structure uses both a global clock (CLK) and its logical inverse (CLKB).

**TABLE 1: COMBINATORIAL LOGIC VERSUS SEQUENTIAL LOGIC**

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic function generation</td>
<td>Capture and holds state of combinational logic</td>
</tr>
<tr>
<td>SET: Glitch in the combinational logic: Capture is frequency dependent</td>
<td>SEU: Next state capture can be frequency dependent</td>
</tr>
<tr>
<td>Double-sided</td>
<td>Single-sided</td>
</tr>
</tbody>
</table>

1) **Synchronous Design Concepts and the Functional Data Path**

The essence of synchronous design considers DFFs as boundary points. In a design, each boundary point DFF will have a cone of logic feeding it. The cone is defined to be a backwards trace from an End-Point DFF that stops at its previous stage DFFs (Start-Point DFFs). The trace includes the Start-Point DFFs and all combinational logic within the path. One cone of logic is illustrated in Fig. 1.

![Fig. 1 Start-Point DFFs to End-Point DFFs](image)

2) **P(fs) \_ functionalLogic Evaluation for Synchronous Designs**

In order to analyze \( P(fs) \_ functionalLogic \), each DFF is evaluated as an End-Point with a cone of logic backwards trace. \( \tau_{dy} \) is the delay from a Start-Point DFF to an End-Point DFF within a cone of logic. There is a unique \( \tau_{dy} \) for every Start-Point to End-Point. By definition of synchronous design: \( \tau_{dy} < \tau_{clk} \).

Equation (4) is a breakdown of \( P(fs) \_ functionalLogic \) by Start-Point DFF and combinational logic.

**TABLE 2: DEFINITION OF TERMS IN EQUATION 4**

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{DFFSEU} )</td>
<td>Probability that the Start-Point DFF will incur a SEU and that it will be captured by an End-Point</td>
</tr>
<tr>
<td>( P_{SET} )</td>
<td>Probability that the Start-Point DFF will incur a SET and it will be captured by an End-Point</td>
</tr>
</tbody>
</table>

\[
P(fs) \_ functionalLogic = \sum_{DFF} \left( \sum_{j=1}^{\#StartPointDFFs} P(fs) \_ DFFSEU \_ SET(\cdot) + \sum_{i=1}^{\#CombinationalCells} P(fs) \_ SET \_ SEU(\cdot) \right)
\]

3) **Capturing Start-Point DFF Upsets (P(fs) \_ DFFSEU \_ SEU)**

![Fig. 2: Will the End-Point DFF capture the Start-Point SEU? Capture occurs if \( 0 < t < (\tau_{clk} - \tau_{dy}) \) giving the one-sided signal enough time to reach the End-Point DFF](image)

**TABLE 3: DEFINITION OF TERMS**

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{DFFSEU} )</td>
<td>Probability the Start-Point DFF will incur a SEU</td>
</tr>
<tr>
<td>( 1 - \tau_{dy} _ fs )</td>
<td>Portion of clock cycle that the End-Point DFF can capture a Start-Point DFF SEU before the next clock edge.</td>
</tr>
<tr>
<td>( \tau_{dy} )</td>
<td>Assumes the SEU Start-Point DFF is always enabled and will have a valid value at the next clock edge</td>
</tr>
<tr>
<td>( P_{SET} )</td>
<td>Probability a combinational gate will incur a SET</td>
</tr>
<tr>
<td>( P_{prop} )</td>
<td>Probability the SET can propagate to an End-Point DFF</td>
</tr>
</tbody>
</table>

If a Start-Point DFF incurs a SEU ($P_{DFFSEU}$) it will occur at time $\tau$ as a single sided function (see Table 1) somewhere within a clock period ($t_{clk}$). It will not manifest as a system upset unless an End-Point DFF captures the single sided upset at the next clock edge. An End-Point will only capture the Start-Point upset if it occurs at $\tau$ such that after propagating through the delay path ($t_{dy}$), the single sided upset arrives at the data pin of the End-Point prior to the clock edge as shown in Fig. 3 and (5).

$$\tau < t_{clk} - t_{dy}$$

The portion of the clock period that a Start-Point DFF SEU can be captured by an End-Point DFF is shown (6).

$$\frac{\tau}{t_{clk}} = 1 - \frac{t_{dy} \cdot f_s}{1 - t_{dy} \cdot f_s}$$

The probability that $P_{DFFSEU}$ will manifest as a system error ($P_{DFFSEU->SEU}$) is reflected (7).

$$P(f_s)_{DFFSEU->SEU} \propto \sum_{DFF} \left( \#StartPointDFFs \cdot P_{DFFSEU}(j) \cdot (1 - t_{dy}(j) \cdot t_{width}(j) \cdot f_s) \right)$$

4) System Upsets due Combinatorial logic ($P_{SET->SEU}$)

If a SET occurs in a combinatorial logic gate within the cone of logic for an End-Point DFF, it has the possibility of being captured by its End-Point with a probability of ($P(f_s)_{SET->SEU}$). It has been shown [1][2] that the upper-bound $P(f_s)_{SET->SEU}$ for a synchronous design is proportional to the following probabilities: generation of a SET ($P_{gen}$), propagation of the SET ($P_{prop}$), and capture of the SET. In addition, the SET capture is proportional to the width ($t_{width}$) of the SET with respect to the $f_s$ as shown in (8).

$$P_{SET->SEU} \propto \sum_{DFF} \left( \#CombinatorialCells \cdot \sum_{i=1}^{\#CombinatorialCells} (P_{gen}(i) \cdot P_{prop}(i) \cdot t_{width}(i) \cdot f_s) \right)$$

5) Putting it all together DFF and Combinatorial Logic Upsets

As previously mentioned, data path susceptibility ($P(f_s)_{functionalLogic}$) is based on the cone of logic Start-Point DFF capture ($P(f_s)_{DFFSEU->SEU}$) and combinatorial logic gate capture ($P(f_s)_{SET->SEU}$) as shown in (9).

C. Single Event Functional Interrupt ($P_{SEFI}$)

A Single Event Functional Interrupt (SEFI) is a SEU that forces the FPGA to be inoperable. According to the NASA REAG SEU Model, $P_{SEFI}$ has two major categories:

1) Global Route SEFI: $P_{GlobalRoutes}$

As previously mentioned, in a synchronous design, all DFFs must be connected to a clock. In addition, all DFFs should be connected to a reset. Clock and reset signals are categorized as global routes because they are connected to a large number of components. An upset in a global route can cause catastrophic events because a large number of elements can be affected simultaneously. Subsequently, global route networks have been categorized as a SEFI.

2) Hidden Logic SEFI: $P_{hiddenLogic}$

Some FPGA devices have additional logic that are inaccessible to the designer. The hidden logic is used for a variety of operations depending on the manufacturer. The ProASIC3 and RTAXS contain JTAG circuitry [4][6]. If the circuitry were to incur a SEU, it is possible for the FPGA's I/O to become inoperable and hence cause catastrophic responses, i.e. a SEFI. However, if the circuitry is grounded during operation, it has been proved that no SEFIs are possible [4][6].

3) ProASIC3 and RTAXS $P_{SEFI}$ Equation

Regarding the ProASIC3 and RTAXS FPGA devices, the hidden logic contribution to $P_{SEFI}$ is considered zero. Hence, $P_{SEFI}$ is only affected by the FPGA design’s global routes.

$$P_{ProASIC3 and RTAXS: SEFI} \propto P_{GlobalRoutes}$$

III. ANALYSIS OF MODEL COMPONENTS

It is intuitive to expect that a non-mitigated design will have a significantly higher $\sigma_{SEU}$ than a mitigated design. It is not necessarily intuitive to determine the strength of the mitigation or the dominant source of SEUs. However, component significance can be determined using Table 4 and $\sigma_{SEU}$ data.

TABLE 4: ANALYSIS OF SEU CAPTURE EFFECTS: $P_{DFFSEU->SEU}$ VERSUS $P_{SET->SEU}$

<table>
<thead>
<tr>
<th>Logic</th>
<th>DFF Capture</th>
<th>Combinatorial SET Capture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capture percentage of clock period</td>
<td>$1 - t_{dy}/t_{clk}$ = \text{As frequency increases, } P_{DFFSEU-&gt;SEU} \text{ increases}</td>
<td>$1 - t_{dy}/t_{clk}$ = \text{As frequency increases, } P_{SET-&gt;SEU} \text{ increases}</td>
</tr>
</tbody>
</table>

Based on Table 4, the following is a list of trends used for evaluating \( \sigma_{\text{SEU}} \) data and determining dominant sources of susceptibility:

\[
P_{(fs)}_{\text{OFF∪SEU}} \quad \text{Dominance - Most SEUs stem from Captured Start-Point DFFs. This is true when:} \\
- \text{There is an increase in the number of combinatorial logic blocks or } \tau_{\text{di}} \text{ and the } \sigma_{\text{SEU}} \text{ } (P_{(fs)}_{\text{error}}) \text{ decreases in response} \\
- \text{There is an increase in frequency and the } \sigma_{\text{SEU}} \text{ decreases in response} \\
\]

\[
P_{(fs)}_{\text{SET∪SEU}} \quad \text{Dominance - Most SEUs stem from Captured Combinatorial Logic SETs. This is true when:} \\
- \text{There is an increase in frequency and } \sigma_{\text{SEU}} \text{ increases in response} \\
- \text{There is an increase in combinatorial logic and } \sigma_{\text{SEU}} \text{ increases in response} \\
\]

Local Mitigation Strength: If the design has been mitigated using a localized-DFF mitigation scheme such as Localized Triple Modular Redundancy (LTMR)[1] or Dual Inter Cell (DICE)[6]:

- It is expected that the DFFs are masked from \( \sigma_{\text{SEU}} \) contribution. \( P_{(fs)}_{\text{OFF∪SEU}} \) should be insignificant and hence \( \sigma_{\text{SEU}} \) is lower.
- However, if \( P_{(fs)}_{\text{OFF∪SEU}} \) has the most significant error contribution for a localized-DFF mitigation scheme, then the mitigation scheme is considered weak because it is not fully masking DFF upsets.

IV. REDUCING SYSTEM ERROR: TRIPLE MODULAR REDUNDANCY SCHEMES

Before testing is performed, general models of expected SEU probabilities based on mitigation and device logic structure are constructed. The models are used as reference points during radiation testing. During the analysis phase, the models are refined to reflect SEU results from radiation testing.

For the ProASIC3 and RTAXS, as previously mentioned, \( P_{\text{configuration}} \) is near zero. Substituting \( P_{(fs)}_{\text{OFF∪SEU}} \) and \( P_{(fs)}_{\text{SET∪SEU}} \) in (1) for \( P_{(fs)}_{\text{functionalLogic}} \), a non-mitigated ProASIC3 or RTAXS design is expected to have a \( \sigma_{\text{SEU}} \) cross as reflected in (11).

\[
\begin{align*}
\text{No - Mitigation } \sigma_{\text{SEU}}: \\
P_{(fs)}_{\text{error}} & \approx P_{\text{OFF∪SEU}} + P_{\text{SET∪SEU}} + P_{\text{SEFI}} \\
\end{align*}
\]

In order to reduce \( \sigma_{\text{SEU}} \), mitigation is applied to the FPGA design. A common form of mitigation is Triple Modular Redundancy (TMR). TMR is a scheme such that a group of circuitry is triplicated and then voted. The mitigation is a majority voter i.e. best-two-out-of-three. It is important to differentiate and signify the TMR scheme based on which circuits are redundant so that the user is aware of the strength of the mitigation strategy. The following is a discussion of two TMR schemes: Localized TMR (LTMR) and Distributed TMR (DTMR).

A. Localized TMR (LTMR)

![LTMR Diagram](image)

LTMR is the process of triplicating each DFF of a design and inserting a voter after each DFF triplication [1][7]. The LTMR process is illustrated in Fig 3. A limitation of LTMR is that shared data paths exist as inputs to the triplicated DFFs. Consequently data path SETs are not mitigated and have the ability to be captured [1][2][5].

As a synopsis of the mitigation power of ProASIC3 and RTAXS LTMR, DFFs (\( P_{\text{OFF∪SEU}} \)) are mitigated, but data paths (\( P_{\text{SET∪SEU}} \)) are not. If follows that (11) is reduced to (12) with LTMR insertion.

\[
\text{LTMR } \sigma_{\text{SEU}}: P_{(fs)}_{\text{error}} \propto P_{\text{SET∪SEU}} + P_{\text{SEFI}}
\]

B. Distributed TMR (DTMR)

![DTMR Diagram](image)

Fig 4 Distributed Triple Modular Redundancy (DTMR). The entire design is triplicated and a voter is inserted into each of the data paths.

DTMR is the process of triplicating the entire design [1][7] excluding global routes such as clocks, resets, and global enables. DTMR is illustrated in Fig 4. No shared data paths exist. The points of susceptibility are only attributed to the global routes (or manufacturer hidden logic). In this manuscript global routes have been grouped into PSRN. Accordingly, the DTMR mitigation strategy is expected to reduce (11) to (13). Due to the dominance of \( P_{SEF} \) in DTMR circuits, DTMR becomes a prime method for evaluating global routes during SEE testing.

\[
\text{DTMR } \sigma_{SEU} : P(f_S) \propto P_{SEF} 
\]  

(13)

V. PROASIC3 AND RTAXS SEE TEST STRUCTURES

The Device-Under-Test (DUT) test structures followed the NASA REAG FPGA testing methodology [2] implementing Windowed Shift Registers (WSR) strings and Counter Arrays. Only data pertaining to WSR chains are presented.

\[
\begin{align*}
\text{WSR}_0 & \quad \text{Average } \tau_{\text{dly}} \approx 1\text{ns} \\
\text{WSR}_8 & \quad \text{Average } \tau_{\text{dly}} \approx 7.5\text{ns}
\end{align*}
\]

Fig. 5 Windowed Shift Register (WSR)

A WSR is a shift register with a different output scheme as illustrated in Fig. 5. Instead of outputting the last DFF once every clock cycle, a WSR outputs the last 4 DFFs once every 4 clock cycles. The parallel output has proven successful for high speed transmission [1].

Windowed Shift Register (WSR) Nomenclature
- \( \text{WSR}_0 \): N=0 Chain ... Only DFFs
- \( \text{WSR}_8 \): N=8 Chain... 8 Inverters per 1 DFF
- \( \text{WSR}_\text{16} \): N=16 Chain... 16 Inverters per 1 DFF

Fig. 6: Theoretical representation of one stage of a WSR chain. Actual WSR FPGA implementation general has additional combinatorial logic within each stage. Average \( \tau_{\text{dly}} \text{WSR}_0 \approx 1\text{ns} \) and Average \( \tau_{\text{dly}} \text{WSR}_8 \approx 7.5\text{ns} \)

Fig. 6 is a schematic representation of one stage of a WSRs and WSRs shift register. Test structure WSR chains contain hundreds of stages per WSR string [5] in order to increase event statistics during SEE testing.

It is important to note that although WSR0 represents a WSR with only DFFs, in actual FPGA implementations, a small portion of additional-unexpected combinatorial logic can exist within the shift register stages. The additional logic is not shown in Fig. 6.

Static Timing Analysis (STA) has been performed on the WSR test structures. STA indicates that the average \( \tau_{\text{dly}} \) for \( \text{WSR}_0 \left( \tau_{\text{dly}} \text{WSR}_0 \right) \approx 1\text{ns} \) and the average \( \tau_{\text{dly}} \) for \( \text{WSR}_8 \left( \tau_{\text{dly}} \text{WSR}_8 \right) \approx 7.5\text{ns} \).

The LTMR and DTMR ProASIC3 designs have been inserted using the automated synthesis tool: Mentor Precision-RTL [7].

VI. HEAVY ION SEE TESTING

Heavy-ion testing has been performed at Texas A&M using the NASA REAG Low Cost Digital Testing (LCDT) System[4][5].

A. SEE Cross Section Calculation

While the ProASIC3 is exposed to an active heavy-ion beam, designs are operating and outputs are compared to expected values for each clock cycle. If an output is not equivalent to its expected state, then an upset is recorded. \( \sigma_{SEU} \) are based on the number of observed upsets normalized by the active beam particle fluence. Depending on the evaluation, an additional normalization step may be implemented to enhance analysis.

B. WSR Chains

Each WSR chain (e.g. \( N=0 \), \( N=8 \), and \( N=16 \)) has a unique SEE cross section (\( \sigma_{\text{WSR}_N \_SEU} \)) and is normalized by the number of DFFs (bits) contained in the string. Equation (14) shows \( \sigma_{\text{WSR}_N \_SEU} \).

\[
\sigma_{\text{WSR}_N \_SEU} = \frac{\text{WSR Upsets}}{\text{#Particles} \cdot \#\text{WSR_D FFs bits}} \quad \left[ \text{cm}^2 \right] 
\]

(14)

C. Global Routes

Because global routes are connected to multiple DFF cells, one upset can affect a significant number of DFFs. Subsequently, global routes are not normalized by bit. SEE cross sections are measured by device. Equation (15) shows \( \sigma_{\text{SEF}} \).

\[
\sigma_{\text{SEF}} = \frac{\text{Global Route}}{\text{#Particles}} \quad \left[ \text{cm}^2 \right] 
\]

(15)

D. SEE Cross Section Analysis

After the SEE cross sections are calculated, comparisons are performed to their expected models and across designs. WSRs are evaluated to determine:
- \( P(\beta)_{\text{DFF-SEU}} \) versus \( P(\beta)_{\text{SET-SEU}} \) dominance: Which elements mostly contribute to the overall \( \sigma_{SEU} \) DFFs or combinatorial logic?
- Frequency dependency: Is there a strong \( P_{\text{SET-SEU}} \) component? If frequency dependence is significant, frequency based \( \sigma_{SEU} \) data should be used as input to error rate calculations.
- Other SEE Model effects and trends as previously described in Section III.

VII. HEAVY ION TEST RESULTS AND ANALYSIS

A. ProASIC3 Analysis

One would expect that WSR₈ σ_SEU (σ_WS₈_SEU) will always be greater than WSR₀ σ_SEU (σ_WS₀_SEU) because WSR₈ chains have more logic. However, σ_SEU data reveals that this is not always a valid assumption. Fig. 7 illustrates that for ProASIC3 No-TMR WSRs, σ_WS₀_SEU > σ_WS₈_SEU across all LETs.

Why are No-TMR ProASIC3 σ_WS₀_SEU > σ_WS₈_SEU for every LET? Consider τ_d/τ. With No-TMR, the DFFs are not mitigated. Hence P_DFFSEUSET > 0 and there is a τ_d/τ dependence. It is known that:

τ_d/τ_WS₀ < τ_d/τ_WS₈ (Fig. 6) and σ_SEU ∝ (1-τ_d/τ) (as shown in (7)), hence it follows that No-TMR: σ_WS₀_SEU > σ_WS₈_SEU.

This can be further observed using the REAG FPGA SEU Model and σ_SEU data. Equation (16) reflects the σ_SEU heavy ion data in Fig. 7 and the fact that σ_WS₀_SEU > σ_WS₈_SEU:

\[
P(\text{DFFSEUSET}) > P(\text{DFFSEUSET}) + P(\text{SETSEU})\]

Equation (17) to form (18):

\[
P(\text{DFFSEUSET}) > P(\text{DFFSEUSET}) + \sum_{i=1}^{8} P(f_s)_{\text{SETSEU(i)}} \]

Equation (18) reveals the τ_d/τ dependence with respect to the σ_SEU. In addition, rearrangement (18) leads to (19) and shows that DFFs are more SEU susceptible than combinatorial logic.

\[
P(\text{DFFSEUSET}) > \frac{\tau_{dl}}{\tau_{dr}} \sum_{i=1}^{8} P(f_s)_{\text{SETSEU(i)}} \]

Fig. 8: Ratio of ProASIC3 No-TMR WSR₀ to WSR₈ σ_SEU across LET

A more detailed inspection of relative σ_SEU's for the ProASIC3 No-TMR WSR₀ and WSR₈ is illustrated in Fig. 8. It can be seen that as LET increases, the ratio of WSR₀ to WSR₈ slightly decreases. This can be explained using (17) or (18). As LET increases, SETs increase in significance. Consequently, the P(f_s)SETSEU component becomes more significant and subsequently reduces the relative difference between σ_WS₀_SEU and σ_WS₈_SEU.

B. ProASIC3 LTMR-WSRs: P_SETSEU

Fig. 9: ProASIC3 LTMR WSR₀, WSR₈, and...
and the effects of (18), the following hold true for LTMR ProASIC3 designs:

- As the number of combinatorial logic gates increases, $P(fs)_{SET-SEU}$ increases and hence $\sigma_{SEU}$ increases. i.e. LTMR $\sigma_{WSRO_SEU} < \sigma_{WSRn_SEU}$, as illustrated in Fig. 7.
- As frequency increases, $\sigma_{WSRn_SEU}$ also increases, as illustrated in Fig. 9.

C. ProASIC3 versus RTAXS Analysis

1) RTAXS Embedded LTMR versus LTMR-ProASIC3

Fig. 10 is a comparison between RTAXS WSRs (contains embedded LTMR) with the ProASIC3 WSRs (contains user inserted LTMR). It is shown that although the RTAXS has an overall lower $\sigma_{SEU}$, the LTMR'd ProASIC3 $\sigma_{SEU}$ are not drastically higher. In addition, the data shows that the LET threshold (LET$_{TR}$) for the LTMR'd ProASIC3 is statistically similar to the RTAXS.

![Fig. 10](image)

ProASIC3 $\sigma_{WSRn_SEU}$ are higher than RTAXS $\sigma_{WSRn_SEU}$ for two major reasons:

1. The ProASIC3 is a commercial grade part containing gates with switching rates considerably higher than the RTAXS[4][6]. In addition, the routing network of the ProASIC3 has less capacitive loading than the RTAXS as fan-out and length increases. By definition, faster switching rates and less capacitance lead to a higher SET $P_{SET}$ than slower circuits that contain significant capacitive loading.

2. The RTAXS embedded mitigation scheme uses a wired-or as a voter[3][4]. The wired-or does not contribute to the $\sigma_{SEU}$ because it does not use transistors to perform the voting. However, the ProASIC3 voters utilize a number of transistors to perform the "best-two-out-of-three function and hence have a significant contribution to the overall $\sigma_{SEU}$. Fig. 6 illustrates the difference between RTAXS and ProASIC3 mitigation schemes.

Table 5 provides the variation in factors that influence the \( \sigma_{WSDR,SEU} \) response for No-TMR ProASIC3 and RTAXS WSRs.

D. DTMR ProASIC3 Results and \( P_{SEFI} \)

Equation (13) shows that DTMR mitigates all of \( P(f/s)_\text{combinational} \) forcing \( P_{SEFI} \) to be the dominant \( \sigma_{SEU} \). Subsequently, DTMR FPGA designs facilitate test and analysis of \( P_{SEFI} \).

![Global Upsets with DTMR](image)

Fig. 12: DTMR WSR Global Route SEU Cross Sections operating at 50MHz and 1MHz with checkerboard data pattern. Cross Sections are per device. No Global SEUs were observed below LET = 20.3 MeV·cm²/mg at 50MHz.

It is noted that no global route upsets were observed below 53.1 MeV·cm²/mg for WSR strings. However, for more complex test structures, global route upsets were observed at 20.3 MeV·cm²/mg and above [5]. More testing is expected to be completed to increase statistics and enhance ProASIC3 global route analysis.

Global routes are expected not to have a frequency dependence because they are not captured SEUs. However, they can cause a SEU to be captured. As an example, a SET that occurs on a global route (e.g., a clock) can cause a DFF to capture the state of its data pin at an erroneous point in time regardless of clock frequency. The \( \sigma_{SEU} \) data reflects this assumption and does not show frequency dependence.

As previously mentioned, global routes are designed to connect to a large number (tens of thousands) of DFF clock or reset pins. Generally, their routing structures are accomplished as a tree of buffers [1][4][6]. The buffers are required to have switching rates (rise-fall times) in the picoseconds range while driving a considerable capacitive load. The \( \sigma_{SEU} \) data in Fig. 12 shows a relatively high LET TH for global routes. This suggests that ProASIC3 global networks have an inherent hardness due to their high-drive capability and capacitive damping throughout their routes.

VIII. CONCLUSION

The NASA REAG FPGA SEU testing methodology has been applied to Actel RTAXS and ProASIC3 FPGA devices. Because the ProASIC3 is a commercial grade device, mitigation strategies have been inserted into the DUT designs. Each design with and without mitigation has been evaluated to determine the effectiveness of the various mitigation strategies.

During the development and test phases, high level REAG FPGA SEU models assisted with DUT design creation and were used as points of reference during testing. Post-irradiation, SEU test results were analyzed and applied to the expected SEU probability models to develop more precise models. The refined FPGA SEU models have proven to reliably reflect the \( \sigma_{SEU} \) data, mitigation strategy, and synchronous design component effects (DFFs and combinatorial logic).

Regarding heavy-ion data, ProASIC3 LTMR has proven to improve SEU performance with respect to No-TMR ProASIC3 designs by increasing the \( \text{LET}_{TH} \) to near 8.6 MeV·cm²/mg and reducing the overall \( \sigma_{SEU} \).

When comparing the LTMR ProASIC3 to the RTAXS SEU data, it has been shown that the ProASIC3 LTMR LET Threshold (\( \text{LET}_{TH} \)) is compatible with the RTAXS \( \text{LET}_{TH} \). However, the overall ProASIC3 LTMR cross sections are higher than the RTAXS cross sections. In addition, \( \sigma_{SEU} \) reduction was observed as the number of combinatorial logic blocks were increased for both devices. However, it has been shown that the cause for the \( \sigma_{SEU} \) reduction in both devices and when it occurs are due to completely different conditions.

Using the REAG FPGA model illustrated why DTMR isolates \( P_{SEFI} \) and subsequently is an effective method for test and evaluation of \( P_{SEFI} \). Heavy ion data show that ProASIC3 DTMR has improved the SEU response by increasing \( \text{LET}_{TH} \) to near 20 MeV·cm²/mg.

The testing methodology developed by NASA REAG
includes test preparation, test execution, and data analysis. The approach has proven to be a successful, technology-independent means to facilitate device evaluation and comparison studies.

REFERENCES

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