Incorporating Probability Models of Complex Test Structures to Perform Technology Independent FPGA Single Event Upset Analysis

M. Berg, Member IEEE, H. Kim, M. Friendlich, C. Perez, C. Seidleck, K. LaBel, Member IEEE

Abstract—We present SEU test and analysis of the Microsemi ProASIC3 FPGA. SEU Probability models are incorporated for device evaluation. Included is a comparison to the RTAXS FPGA illustrating the effectiveness of the overall testing methodology.

Index Terms—FPGA, ProASIC3 versus RTAXS, SEU, Test and Analysis

I. INTRODUCTION

A n effective method for modeling Single Event Upset (SEU) probabilities \( P(f_{\text{error}}) \) in Field Programmable Gate Array (FPGA) devices has been presented[1][2]. It is a top-down modeling approach. The top-level of the FPGA \( P(f_{\text{error}}) \) model was shown to have three major components (1):

- Configuration SEU cross section \( P_{\text{configuration}} \)
- Data path or functional logic SEU cross section \( P_{\text{Functional Logic}} \)
- Single Event Functional Logic SEU cross section \( P_{SEFI} \)

\[
P(f_{\text{error}}) \propto P_{\text{configuration}} + P_{\text{Functional Logic}} + P_{SEFI}
\]  

The SEU Probability model is used by NASA Goddard Radiation Effects and Analysis Group (REAG) as a Single Event Effects (SEE) data analysis tool. Upsets that occur during radiation testing are differentiated and are categorized in order to enhance device evaluation. The model is a reflection of the SEU cross section \( \sigma_{\text{SEU}} \) for a synchronous digital system. Operational frequency \( f_s \) is understood to be the inverse of clock period \( \tau_{\text{clk}} \) as in (2).

\[
\tau_{\text{clk}} = \frac{1}{f_s}
\]  

The importance of this subject matter is to present Microsemi ProASIC3 FPGA SEU behavior under a variety of conditions while illustrating how the REAG SEU model facilitates a detailed analysis that spans across FPGA device technologies. Microsemi RTAXS data[2] will be used as a comparison.

II. \( P(f_{\text{error}}) \) MODEL COMPONENTS

Before radiation testing is performed, models of expected SEU probabilities based on mitigation and device logic structure are constructed. The models are used as reference points during radiation testing. During the analysis phase, the models are refined to reflect SEU results from radiation testing. The following is a more detailed discussion of each element in (1).

A. FPGA Configuration and \( P_{\text{configuration}} \)

Configuration is a separate technology than the functional logic. Accordingly, it has its own categorization of upsets. It has been shown through Configuration SEE radiation testing of Antifuse[1]-[4] and Flash technologies[3][4] that \( P_{\text{configuration}} \) is considered zero as in (3).

Antifuse and Flash Configuration:

\[
P_{\text{configuration}} \to 0
\]  

The RTAXS has an antifuse configuration [7] while the ProASIC3 has a flash configuration [8]. Because \( P_{\text{configuration}} \) is essentially zero for these devices, the following discussion focuses on \( P(f_{\text{error}})_{\text{Functional Logic}} \) and \( P_{SEFI} \).

B. Functional Logic Data Path Upsets and \( P_{\text{Functional Logic}} \)

The functional logic data path is comprised of: Combinatorial Logic, Flip-Flops (DFFs), and Routes. Table 1 illustrates upset types that can potentially occur in a FPGA data path. In a synchronous design, every DFF is connected to a global clock signal. Because a DFF is master-slave edge
flip-flop its internal structure uses both a global clock (CLK) and its logical inverse (CLKB).

**TABLE 1: COMBINATORIAL LOGIC VERSUS SEQUENTIAL LOGIC**

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic function generation</td>
<td>Captures and holds state of combinational logic</td>
</tr>
<tr>
<td>SET: Glitch in the combinational logic: Capture is frequency dependent</td>
<td>SEU: Next state capture can be frequency dependent</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Double-sided</td>
<td>Single-sided</td>
</tr>
</tbody>
</table>

1) Synchronous Design Concepts and the Functional Data Path

The essence of synchronous design considers DFFs as boundary points. In a design, each boundary point DFF will have a cone of logic feeding it. The cone is defined to be a backwards trace from an End-Point DFF that stops at its previous stage DFFs (Start-Point DFFs). The trace includes the Start-Point DFFs and all combinational logic within the path. One cone of logic is illustrated in Fig. 1.

![Cone of Logic](image)

Fig. 1 Start-Point DFFs \rightarrow End Point DFFs \tau_{dy} and the Cone of Logic

2) \( P(\text{fs})_{\text{functionalLogic}} \) Evaluation for Synchronous Designs

In order to analyze \( P(\text{fs})_{\text{functionalLogic}} \), each DFF is evaluated as an End-Point with a cone of logic backwards trace. \( \tau_{dy} \) is the delay from a Start-Point DFF to an End-Point DFF within a cone of logic. There is a unique \( \tau_{dy} \) for every Start-Point to End-Point. By definition of synchronous design: \( \tau_{dy} < \tau_{clk} \).

Equation (4) is a breakdown of \( P(\text{fs})_{\text{functionalLogic}} \) by Start-Point DFF and combinational logic.

**TABLE 2: DEFINITION OF TERMS IN EQUATION 4**

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{\text{OFF-SEU}} )</td>
<td>Probability that the Start-Point DFF will incur a SEU and that it will be captured by an End-Point</td>
</tr>
<tr>
<td>( P_{\text{SET-SEU}} )</td>
<td>Probability that the Start-Point DFF will incur a SEU and it will be captured by an End-Point</td>
</tr>
</tbody>
</table>

\[
P(\text{fs})_{\text{functionalLogic}} = \exists_{DFF} \left( \sum_{j=1}^{\#\text{StartPointDFFs}} P(\text{fs})_{DFFSEU \rightarrow SEU(j)} + \sum_{i=1}^{\#\text{CombinationalCells}} P(\text{fs})_{\text{SET} \rightarrow \text{SEU}(i)} \right) \quad (4)
\]

3) Capturing Start-Point DFF Upsets (\( P(\text{fs})_{DFFSEU \rightarrow SEU} \))

**TABLE 3: DEFINITION OF TERMS**

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{\text{OFF-SEU}} )</td>
<td>Probability the Start-Point DFF will incur a SEU</td>
</tr>
<tr>
<td>( 1 \cdot \tau_{dy,fs} )</td>
<td>Portion of clock cycle that the End-Point DFF can capture a Start-Point DFF SEU before the next clock edge. Assumes the SEU Start-Point DFF is always enabled and will have a valid value at the next clock edge</td>
</tr>
<tr>
<td>( P_{\text{prop}} )</td>
<td>Probability a combinational gate will incur a SET</td>
</tr>
<tr>
<td>( P_{\text{prop}} )</td>
<td>Probability the SET can propagate to an End-Point DFF</td>
</tr>
</tbody>
</table>

If a Start-Point DFF incurs a SEU ($P_{OFFSEU}$) it will occur at time $\tau$ as a single sided function (see Table 1) somewhere within a clock period ($t_{clk}$). It will not manifest as a system upset unless an End-Point DFF captures the single sided upset at the next clock edge. An End-Point will only capture the Start-Point upset if it occurs at $\tau$ such that after propagating through the delay path ($t_{dly}$), the single sided upset arrives at the data pin of the End-Point prior to the clock edge as shown in Fig. 3 and (5).

$$\tau < t_{clk} - t_{dly} \tag{5}$$

The portion of the clock period that a Start-Point DFF SEU can be captured by an End-Point DFF is shown (6).

$$\frac{\tau}{t_{clk}} < 1 - \frac{t_{dly}}{t_{clk}} = 1 - t_{dly}/t_{fs} \tag{6}$$

The probability that $P_{OFFSEU}$ will manifest as a system error ($P_{OFFSEU \rightarrow SEU}$) is reflected (7).

$$P(f_s)_{OFFSEU \rightarrow SEU} \propto \sum_{j=1}^{\#StartPointDFFs} P_{OFFSEU(j)}(1 - t_{dly(j)f_s}) \tag{7}$$

4) System Upsets due Combinatorial logic ($P_{SET \rightarrow SEU}$)

If a SET occurs in a combinatorial logic gate within the cone of logic for an End-Point DFF, it has the possibility of being captured by its End-Point with a probability of ($P(f_s)_{SET \rightarrow SEU}$). It has been shown [1][2] that the upper-bound $P(f_s)_{SET \rightarrow SEU}$ for a synchronous design is proportional to the following probabilities: generation of a SET ($P_{gen}$), propagation of the SET ($P_{prop}$), and capture of the SET. In addition, the SET capture is proportional to the width ($t_{width}$) of the SET with respect to the $t_{fs}$ as shown in (8).

$$P_{SET \rightarrow SEU} \propto \sum_{i=1}^{\#CombinatorialCells} P_{gen(i)} P_{prop(i)} t_{width(i)} f_s \tag{8}$$

5) Putting it all together DFF and Combinatorial Logic Upsets

As previously mentioned, data path susceptibility ($P(f_s)_{functionalLogic}$) is based on the cone of logic Start-Point DFF capture ($P(f_s)_{OFFSEU \rightarrow SEU}$) and combinatorial logic gate capture ($P(f_s)_{SET \rightarrow SEU}$) as shown in (9).

$$P(f_s)_{functionalLogic} \propto \sum_{j=1}^{\#StartPointDFFs} \sum_{i=1}^{\#CombinatorialCells} P_{OFFSEU(j)}(1 - t_{dly(j)f_s}) P_{prop(i)} t_{width(i)} f_s \tag{9}$$

C. Single Event Functional Interrupt ($P_{SEFI}$)

A Single Event Functional Interrupt (SEFI) is a SEU that forces the FPGA to be inoperable. According to the NASA REAG SEU Model, $P_{SEFI}$ has two major categories:

1) Global Route SEFI: $P_{GlobalRoutes}$

As previously mentioned, in a synchronous design, all DFFs must be connected to a clock. In addition, all DFFs should be connected to a reset. Clock and reset signals are categorized as global routes because they are connected to a large number of components.

An upset in a global route can cause catastrophic events because a large number of elements can be affected simultaneously. Subsequently, global route networks have been categorized as a SEFI.

2) Hidden Logic SEFI: $P_{HiddenLogic}$

Some FPGA devices have additional logic that are inaccessible to the designer. The hidden logic is used for a variety of operations depending on the manufacturer. The ProASIC3 and RTAXS contain JTAG circuitry [4][6]. If the circuitry were to incur a SEU, it is possible for the FPGA's I/O to become inoperable and hence cause catastrophic responses, i.e. a SEFI. However, if the circuitry is grounded during operation, it has been proved that no SEFIs are possible [4][6].

3) ProASIC3 and RTAXS $P_{SEFI}$ Equation

Regarding the ProASIC3 and RTAXS FPGA devices, the hidden logic contribution to $P_{SEFI}$ is considered zero. Hence, $P_{SEFI}$ is only affected by the FPGA design's global routes.

$$P_{SET \rightarrow SEU} \propto P_{GlobalRoutes} \tag{10}$$

III. ANALYSIS OF MODEL COMPONENTS

It is intuitive to expect that a non-mitigated design will have a significantly higher $\sigma_{SEU}$ than a mitigated design. It is not necessarily intuitive to determine the strength of the mitigation or the dominant source of SEUs. However, component significance can be determined using Table 4 and $\sigma_{SEU}$ data.

<table>
<thead>
<tr>
<th>Logic</th>
<th>DFF Capture (%)</th>
<th>Combinatorial SET Capture (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capture percentage of clock period $1 - t_{dly}/t_{fs}$ as frequency increases, $P_{OFFSEU \rightarrow SEU}$ increases</td>
<td>$1 - t_{dly}/t_{fs}$ as frequency increases, $P_{OFFSEU \rightarrow SEU}$ increases</td>
<td></td>
</tr>
</tbody>
</table>

Based on Table 4, the following is a list of trends used for evaluating \( \sigma_{SEU} \) data and determining dominant sources of susceptibility:

- **Increase in frequency** decreases \( P(f)_{OFFSEU-SEU} \) and \( P(f)_{SET-SEU} \).
- **Increase in combinatorial logic** increases \( \tau_{by} \) and decreases \( P(f)_{OFFSEU-SEU} \).

**Local Mitigation Strength:** If the design has been mitigated using a localized-DFF mitigation scheme such as Localized Triple Modular Redundancy (LTMR) [1] or Dual Inter Cell (DICE) [6],

- It is expected that the DFFs are masked from \( \sigma_{SEU} \) contribution. \( P(f)_{OFFSEU-SEU} \) should be insignificant and hence \( \sigma_{SEU} \) is lower.
- However, if \( P(f)_{OFFSEU-SEU} \) has the most significant error contribution for a localized-DFF mitigation scheme, then the mitigation scheme is considered weak because it is not fully masking DFF upsets.

**IV. REDUCING SYSTEM ERROR: TRIPLE MODULAR REDUNDANCY SCHEMES**

Before testing is performed, general models of expected SEU probabilities based on mitigation and device logic structure are constructed. The models are used as reference points during radiation testing. During the analysis phase, the models are refined to reflect SEU results from radiation testing.

For the ProASIC3 and RTAXS, as previously mentioned, \( P_{configuration} \) is near zero. Substituting \( P(f)_{OFFSEU-SEU} \) and \( P(f)_{SET-SEU} \) in (1) for \( P(f)_{functionalLogic} \), a non-mitigated ProASIC3 or RTAXS design is expected to have a \( \sigma_{SEU} \) cross as reflected in (11).

\[
No - Mitigation \sigma_{SEU}:
\]

\[
P(f)_{error} \propto P(f)_{OFFSEU-SEU} + P(f)_{SET-SEU} + P_{SEFI}
\]

B. Distributed TMR (DTMR)

**Fig 4:** Distributed Triple Modular Redundancy (DTMR). The entire design is triplicated and a voter is inserted into each of the data paths.
DTMR is the process of tripling the entire design [1][7] excluding global routes such as clocks, resets, and global enables. DTMR is illustrated in Fig 4. No shared data paths exist. The points of susceptibility are only attributed to the global routes (or manufacturer hidden logic). In this manuscript global routes have been grouped into $P_{SRR}$. Accordingly, the DTMR mitigation strategy is expected to reduce (11) to (13). Due to the dominance of $P_{SRR}$ in DTMR circuits, DTMR becomes a prime method for evaluating global routes during SEE testing.

$$DTMR \sigma_{SSEU} : P(f) \propto P_{SSEU}$$  \hfill (13)

V. PROASIC3 AND RTAXS SEE TEST STRUCTURES

The Device-Under-Test (DUT) test structures followed the NASA REAG FPGA testing methodology [2] implementing Windowed Shift Registers (WSR) strings and Counter Arrays. Only data pertaining to WSR chains are presented.

A WSR is a shift register with a different output scheme as illustrated in Fig. 5. Instead of outputting the last DFF once every clock cycle, a WSR outputs the last 4 DFFs once every 4 clock cycles. The parallel output has proven successful for high speed transmission [1].

Windowed Shift Register (WSR) Nomenclature
- $WSR_0$: $N=0$ Chain... Only DFFs
- $WSR_8$: $N=8$ Chain... 8 Inverters per 1 DFF
- $WSR_{16}$: $N=16$ Chain... 16 Inverters per 1 DFF

$$WSR_0 \text{ Average } \tau_{dy} \approx 1 \text{ ns}$$
$$WSR_8 \text{ Average } \tau_{dy} \approx 7.5 \text{ ns}$$

Fig. 6 is a schematic representation of one stage of a WSR chain. Actual WSR FPGA implementation general has additional combinatorial logic within each stage. Average $\tau_{dy_{WSR}} \approx 1 \text{ ns}$ and Average $\tau_{dy_{WSR}} \approx 7.5 \text{ ns}$

VII. HEAVY ION TEST RESULTS AND ANALYSIS

A. ProASIC3 Analysis

One would expect that WSR₈σₑᵤ ≳ WSR₉σₑᵤ because WSR₈ chains have more logic. However, σₑᵤ data reveals that this is not always a valid assumption. Fig. 7 illustrates that for ProASIC3 No-TMR WSRs, σₑᵤ ≳ WSR₈σₑᵤ across all LETs.

Why are No-TMR ProASIC3 σₑᵤ WSR₈ > WSR₉σₑᵤ for every LET? Consider τₑᵤ. With No-TMR, the DFFs are not mitigated. Hence Pₑᵤ > 0 and there is a τₑᵤ dependence. It is known that:

τₑᵤ < τₑᵤ (Fig. 6) and σₑᵤ ≳(1-τₑᵤ) (as shown in (7)), hence it follows that No-TMR: σₑᵤ > σₑᵤ. This can be further observed using the REAG FPGA SEU Model and σₑᵤ data. Equation (16) reflects the σₑᵤ heavy ion data in Fig. 7 and the fact that σₑᵤ > σₑᵤ:

\[ P(f s)_{\text{DFF} \rightarrow \text{SEU}} > P(f s)_{\text{SET} \rightarrow \text{SEU}} \]  

There is no combinatorial logic in the WSR₉ string; hence the left side of (16) is reduced and forms (17).

\[ P(f s)_{\text{DFF} \rightarrow \text{SEU}} \]  

Substitutions are made for P(fs)DFF→SEU and P(fs)SET→SEU (17) to form (18):

\[ P_{\text{DFF} \rightarrow \text{SEU}} (1 - \frac{\tau_{e,u}}{\tau_{e,k}}) > \]  

Equation (18) reveals the τₑᵤ significance with respect to the σₑᵤ. In addition, rearrangement (18) leads to (19) and shows that DFFs are more SEU susceptible than combinatorial logic.

\[ P_{\text{DFF} \rightarrow \text{SEU}} > \frac{\tau_{e,k}}{\tau_{e,u}} \sum_{i=1}^{8} P(f s)_{\text{SET} \rightarrow \text{SEU}(i)} \]  

A more detailed inspection of relative σₑᵤ’s for the ProASIC3 No-TMR WSR₈ and WSR₉ is illustrated in Fig. 8. It can be seen that as LET increases, the ratio of WSR₈ to WSR₉ slightly decreases. This can be explained using (17) or (18). As LET increases, SETs increase in significance. Consequently, the P(fs)SET→SEU component becomes more significant and subsequently reduces the relative difference between σₑᵤ and σₑᵤ.

B. ProASIC3 LTMR-WSRs: P_SET→SEU

Fig. 7 illustrates that with user-inserted LTMR, the overall σₑᵤ is reduced and now σₑᵤ < σₑᵤ. This is as expected because P(fs)DFF→SEU is mitigated with LTMR. Consequently, with LTMR insertion, P(fs)SET→SEU is now the significant component. In addition the σₑᵤ data in Fig. 7 and Fig. 9 show the dominance of P(fs)SET→SEU for a LTMR design. Given the σₑᵤ data, the dominance of P(fs)SET→SEU.

Fig. 9: ProASIC3 LTMR WSR₈, WSR₉, and WSR₇. As the frequency increases or the number of combinatorial blocks increases, the σₑᵤ increases.

and the effects of (18), the following hold true for LTMR ProASIC3 designs:

- As the number of combinatorial logic gates increases, $P(f)_{SET-SEU}$ increases and hence $\sigma_{SEU}$ increases. i.e. LTMR $\sigma_{WSRO,SEU} < \sigma_{WSRN,SEU}$ as illustrated in Fig. 7
- As frequency increases, $\sigma_{WSRN,SEU}$ also increases, as illustrated in Fig. 9

C. ProASIC3 versus RTAXS Analysis

1) RTAXS Embedded LTMR versus LTMR-ProASIC3

Fig. 10 is a comparison between RTAXS WSRs (contains embedded LTMR) with the ProASIC3 WSRs (contains user inserted LTMR). It is shown that although the RTAXS has an overall lower $\sigma_{SEU}$, the LTMR'd ProASIC3 $\sigma_{SEU}$ are not drastically higher. In addition, the data shows that the LET threshold (LET_TMR) for the LTMR'd ProASIC3 is statistically similar to the RTAXS.

![Graph showing RTAXS versus ProASIC3 100MHz Checkerboard Pattern WSR Strings](image)

**Fig. 10: RTAXS with embedded LTMR versus ProASIC3 with user inserted LTMR, WSR Test Structures**

ProASIC3 $\sigma_{WSRN,SEU}$ are higher than RTAXS $\sigma_{WSRN,SEU}$ for two major reasons:

1. The ProASIC3 is a commercial grade part containing gates with switching rates considerably higher than the RTAXS[4][6]. In addition, the routing network of the ProASIC3 has less capacitive loading than the RTAXS as fan-out and length increases. By definition, faster switching rates and less capacitance lead to a higher SET $P_{SET}$ than slower circuits that contain significant capacitive loading.

2. The RTAXS embedded mitigation scheme uses a wired-or as a voter[3][4]. The wired-or does not contribute to the $\sigma_{SEU}$ because it does not use transistors to perform the voting. However, the ProASIC3 voters utilize a number of transistors to perform the “best-two-out-of-three function and hence have a significant contribution to the overall $\sigma_{SEU}$. Fig. 6 illustrates the difference between RTAXS and ProASIC3 mitigation schemes.

As previously mentioned, one would expect that $\sigma_{WSRO,SEU} < \sigma_{WSRN,SEU}$ because WSR_T has more logic (i.e. WSR_T contains more combinatorial logic between OFF stages than WSR_R). However, we have shown that this is not always the case. In support, Fig. 7 illustrates that across all LET values the No-TMR-ProASIC3 $\sigma_{WSRO,SEU} > \sigma_{WSRN,SEU}$. This No-TMR trend is due to dominant $P(f)_{DFF,SEU}$ and $\tau_{Ry}$. By inserting LTMR, the data shows that the trend reverses. For LTMR-ProASIC3 $\sigma_{WSRO,SEU} < \sigma_{WSRN,SEU}$ for all LET values due to the mitigation of $P(f)_{DFF,SEU}$.

Regarding the SEU response to increasing combinatorial logic in the RTAXS, it has also been observed that an increase in combinatorial logic at LET <10MeV*cm²/mg can reduce $\sigma_{SEU}$ due to attenuation of SETs [2]. Although the RTAXS and the No-TMR ProASIC3 both have trends where $\sigma_{WSRO,SEU} > \sigma_{WSRN,SEU}$, the conditions and rationales for the unexpected SEU response are completely different.

Table 5 provides the variation in factors that influence the $\sigma_{\text{WSR0}} > \sigma_{\text{WSR} \_\text{SEU}}$ response for No-TMR ProASIC3 and RTAXS WSRs.

**Table 5: Comparison of Proofs Explaining Why WSR0 $\sigma_{\text{SEU}}$ < WSR0 $\sigma_{\text{SEU}}$ ProASIC3 versus RTAXS**

<table>
<thead>
<tr>
<th>Significant component</th>
<th>No-TMR ProASIC3</th>
<th>RTAXS Embedded LTMR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Significant circuit type</td>
<td>$P_{\text{off SEU}}(1-t_{\text{off}}/t_{\text{ref}})$</td>
<td>$P_{\text{on SEU}}(t_{\text{on}}/t_{\text{ref}})$</td>
</tr>
<tr>
<td>Error Strength</td>
<td>DFF (sequential): SEU</td>
<td>Combinatorial: SET</td>
</tr>
<tr>
<td>Variables responsible for $\sigma_{\text{SEU}}$</td>
<td>$t_{\text{off}}$ or $t_{\text{on}}/t_{\text{ref}}$</td>
<td>$P_{\text{off SEU}}$ or $P_{\text{on SEU}}$</td>
</tr>
<tr>
<td>LET values when valid</td>
<td>Across all LETs because $t_{\text{off}}$ is constant and $P_{\text{off SEU}}$ remains significant at low LETs</td>
<td>Non-Linear across LET because $P_{\text{off SEU}}$ is weaker as a function of LET</td>
</tr>
</tbody>
</table>

Table 5 shows that the ProASIC3 LTMR mitigates all of the $P_{\text{off SEU}}$ functional properties forcing $P_{\text{off SEU}}$ to be the dominant $\sigma_{\text{SEU}}$. Subsequently, the DTMR FPGA designs facilitate test and analysis of $P_{\text{off SEU}}$.

![Global Upsets with DTMR](Fig.12: DTMR WSR Global Route SEU Cross Sections operating at 50MHz and 1MHz with checkerboard data pattern. Cross Sections are per device. No Global SEUs were observed below LET = 20.3 MeV·cm²/mg at 50MHz. The testing methodology developed by NASA REAG has been applied to Actel RTAXS and ProASIC3 FPGA devices. Because the ProASIC3 is a commercial grade device, mitigation strategies have been inserted into the DUT designs. Each design with and without mitigation has been evaluated to determine the effectiveness of the various mitigation strategies. During the development and test phases, high level REAG FPGA SEU models assisted with DTM design creation and were used as points of reference during testing. Postirradiation, SEU test results were analyzed and applied to the expected SEU probability models to develop more precise models. The refined FPGA SEU models have proven to reliably reflect the $\sigma_{\text{SEU}}$ data, mitigation strategy, and synchronous design component effects (DFFs and combinatorial logic).

Regarding heavy-ion data, the ProASIC3 LTMR has proven to improve SEU performance with respect to No-TMR ProASIC3 designs by increasing the LET$_{\text{TH}}$ to near 8.6 MeV·cm²/mg and reducing the overall $\sigma_{\text{SEU}}$.

When comparing the LTMR ProASIC3 to the RTAXs SEU data, it has been shown that the ProASIC3 LTMR LET Threshold (LET$_{\text{TH}}$) is comparable with the RTAXs LET$_{\text{TH}}$. However, the overall ProASIC3 LTMR cross sections are higher than the RTAXS cross sections. In addition, $\sigma_{\text{SEU}}$ reduction was observed as the number of combinatorial logic blocks were increased for both devices. However, it has been shown that the cause for the $\sigma_{\text{SEU}}$ reduction in both devices and when it occurs are due to completely different conditions.

Using the REAG FPGA model illustrated why DTMR isolates $P_{\text{SEU}}$ and subsequently is an effective method for test and evaluation of $P_{\text{SEU}}$. Heavy ion data show that ProASIC3 DTM has improved the SEU response by increasing LET$_{\text{TH}}$ to near 20 MeV·cm²/mg.

The testing methodology developed by NASA REAG
includes test preparation, test execution, and data analysis. The approach has proven to be a successful, technology-independent means to facilitate device evaluation and comparison studies.

REFERENCES

[1] M. Berg “Trading Application Specific Integrated Circuit (ASIC) and Field Programmable Gate Array (FPGA) Considerations for System Insertion”, NSREC Short Course, Quebec City, CN, July 2009


