NASA GSFC Avionics Architectures and Future Directions

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<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>AI</td>
<td>Artificial Intelligence</td>
<td>GSFC</td>
<td>Goddard Space Flight Center</td>
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<tr>
<td>C&amp;DH</td>
<td>Command and Data Handling</td>
<td>HPSC</td>
<td>High Performance Spaceflight Computing</td>
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<tr>
<td>CAN</td>
<td>Controller Area Network</td>
<td>ICESAT-2</td>
<td>Ice, Cloud, and land Elevation Satellite 2</td>
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<td>cFE</td>
<td>Core Flight Executive</td>
<td>I2C</td>
<td>Inter-Integrated Circuit</td>
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<td>cFS</td>
<td>Core Flight System</td>
<td>IP</td>
<td>Intellectual Property</td>
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<tr>
<td>cPCI</td>
<td>Compact Peripheral Component Interconnect</td>
<td>MUSTANG</td>
<td>Modular Unified Space Technology Avionics for Next Generation</td>
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<tr>
<td>COTS</td>
<td>Commercial Off the Shelf</td>
<td>NASA</td>
<td>National Aeronautics and Space Administration</td>
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<tr>
<td>DET</td>
<td>Direct Energy Transfer</td>
<td>OSAL</td>
<td>Operating System Abstraction Layer</td>
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<td>DSP</td>
<td>Digital Signal Processing</td>
<td>POL</td>
<td>Point Of Load</td>
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<td>EMI</td>
<td>Electromagnetic Interference</td>
<td>PSE</td>
<td>Power System Electronics</td>
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<td>EMC</td>
<td>Electromagnetic Compatibility</td>
<td>PSP</td>
<td>Platform Support Package</td>
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<td>EO-1</td>
<td>Earth Observing 1</td>
<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
<td>RMAP</td>
<td>Remote Memory Access Protocol</td>
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<td>GEDI</td>
<td>Global Ecosystem Dynamics Investigation</td>
<td>RRM3</td>
<td>Remote Refueling Mission 3</td>
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<td>GHz</td>
<td>Gigahertz</td>
<td>SAR</td>
<td>Synthetic Aperture Radar</td>
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<td>GMSA</td>
<td>Goddard Modular Smallsat Architecture</td>
<td>SCEB</td>
<td>Smallsat Common Electronics Board</td>
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<td>GPS</td>
<td>Global Positioning System</td>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
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<td>GPU</td>
<td>Graphics Processing Unit</td>
<td>SRI0</td>
<td>Serial RapidIO</td>
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<td>GN&amp;C</td>
<td>Guidance Navigation and Control</td>
<td>UART</td>
<td>Universal Asynchronous Receiver/Transmitter</td>
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Outline

• NASA GSFC Overview
• Avionics Scope
• Current GSFC Avionics Architectures
• Future Requirements Drivers
• How Future Architectures Can Meet These Needs
• Current Challenges
• NASA’s first Space Flight Center (established 1959)

• Largest Collection of Scientists & Engineers in the U.S.

• Nearly 300 successful missions including the World’s First Weather Satellite and the Hubble Space Telescope

• 2006 Nobel Prize in Physics [Big Bang/Cosmic Background]

• Hubble Space Telescope Supported 2011 Nobel Prize in Physics

=> We TRANSFORM Human Understanding of Earth and Space
Facilities

- GSFC Greenbelt, MD
- GSFC Wallops Flight Facility, VA
- IV&V Facility, WV
- Goddard Institute for Space Studies, NY
- Ground Stations at White Sands Complex, NM
A Diverse Mission Portfolio
Avionics Scope

• The scope of avionics can vary widely across organizations

• For the purposes of this presentation, the scope of avionics is considered to include:
  – Command and Data Handling (C&DH)
  – Power System Electronics (PSE)
  – Guidance Navigation and Control (GN&C)
  – Uplink/downlink (but not the full transponder)
  – Onboard Networks

• Avionics scope does not include science instruments
  – However, avionics components often are used within instrument electronics
Current GSFC Avionics Architectures

- GSFC uses multiple hardware architectures to implement avionics, each targeted for different use cases

<table>
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<tr>
<th>Architecture</th>
<th>Purpose</th>
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<tr>
<td>MUSTANG (Modular Unified Space Technology Avionics for Next Generation)</td>
<td>Command &amp; Data Handling (C&amp;DH) and Power System Electronics (PSE) for medium to large missions</td>
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<tr>
<td>GMSA (Goddard Modular Smallsat Architecture)</td>
<td>Command &amp; Data Handling (C&amp;DH) and Power System Electronics (PSE) for cubesats and smallsats</td>
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<tr>
<td>SpaceCube</td>
<td>High performance onboard processing applications</td>
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Integrated GMSA PSE and C&DH

Global Ecosystem Dynamics Investigation (GEDI) MUSTANG

Robotic Refueling Mission 3 (RRM3) SpaceCube
MUSTANG

- Derived from avionics flown on recent flight missions, MUSTANG targets medium to large missions and instruments

- Employs slice-based architecture, providing a suite of electronic modules that can implement spacecraft avionics and instrument electronics

- Packaging concept has flexibility to accommodate varying slice widths and both single and multi-box configurations

- Uses a dual core GR712C as the primary processor

- Also uses a LEON3FT soft-core processor embedded within an RTG4 FPGA as an auxiliary processor

- Uses SpaceWire/RMAP (Remote Memory Access Protocol) for internal and external communication
MUSTANG

MUSTANG Architecture
• Some existing hardware

- Engine Valve Driver Card
- Digital IO Card
- PSE Monitor Card
- Output Module Card
- Mechanism Control Card
- Housekeeping Card
- Communication Card
- Processor Card
- Deployment Card
- Data Storage Card (Not Fully Populated) Full Capacity 3.5Tb
GMSA

• GMSA targets smallsat and cubesat missions that must operate reliably for long durations in harsh radiation environments

• The GSMA C&DH consists of a Smallsat Common Electronics Board (SCEB) and a mission specific adapter card interconnected via stacking connectors

• The SCEB implements the flight processor as a soft core LEON3FT within a reprogrammable FPGA

• The SCEB also provides UART, I2C, SPI, CAN, and SpaceWire interfaces

• The GSMA PSE consists of 5 cards interconnected via a backplane and uses Direct Energy Transfer (DET) and can support both 3-axis and spin-stabilized spacecraft
• Existing hardware

SCEB

Adapter Board

PSE

Battery Assembly
• SpaceCube is a high performance reconfigurable science/mission data processor based on Xilinx Virtex FPGAs (Field Programmable Gate Arrays)

• The current SpaceCube version 2.0 processor is based on the Virtex-5 FPGA and is implemented as a 3U cPCI board

• Mission specific SpaceCube implementations consist of a processor board along with necessary I/O boards

• SpaceCube allows hybrid processing within the FPGAs
  – Embedded processor cores
  – DSP (Digital Signal Processing) function blocks
  – FPGA logic

• Radiation upset mitigation techniques are employed, including the use of a small “critical function” manager/watchdog

• Multi-gigabit serial interfaces from the FPGAs are brought out as I/O

• SpaceCube “core software” infrastructure includes cFS (Core Flight System) and “SpaceCube Linux” (with Xenomai)
SpaceCube

• Some existing hardware

SpaceCube V2.0
SpaceCube V2.0 Processor Card
Restore-L Video/Spacecraft Interface Card
GPS RF Front-End Interface Card
Across these architectures, GSFC uses Core Flight System (cFS) for flight software:
- A Flight Software Architecture consisting of an OS Abstraction Layer (OSAL), Platform Support Package (PSP), cFE Core, cFS Libraries, and one or more cFS Applications.

**core Flight Executive (cFE)**
- A framework of mission independent, reusable, core flight software services and operating environment.
- Layered on top of, and linked with the OSAL, PSP, and OS.

**cFS App**
- Loosely coupled component using only OSAL, PSP and cFE defined interfaces.

**cFS Library**
- Collection of common application services using only OSAL, PSP, and cFE defined interfaces.
Future Requirements Drivers

• Increased sensor data rates
  – Synthetic Aperture Radar (SAR)
  – Hyperspectral Imagery
  – Lidar
  – Video

• Increased downlink rates
  – Ka-Band
  – Optical
  – Not keeping up with sensor data rates

• Increased onboard science data processing
  – Real-time event/feature detection
  – “Intelligent Instrument” data selection/compression
  – On-board data volume deduction
  – Real-time calibration/correction
  – On-board classification
  – On-board product generation
Future Requirements Drivers

• Autonomous mission applications requiring high bandwidth processing
  – Precision formation flying
  – Autonomous navigation
  – Autonomous rendezvous and docking
  – Terrain relative navigation
  – Real-time sensing and control
  – Real-time image processing

• Improved resource efficiency for small mission classes
  – Tightly integration of spacecraft and instrument functions
  – Share resources between spacecraft and instrument functions where possible

• Distributed space missions with inter-platform collaboration
How Future Architectures Can Meet These Needs

- Use HPSC widely across mission classes
  - Chiplet power, performance, and fault tolerance scalable to meet specific mission needs
  - Middleware significantly reduces the complexity of developing applications for the HPSC Chiplet

- Employ “hybrid processing architectures”, leveraging different compute devices for what they're best suited
  - HPSC Chiplet
  - Graphics Processing Units (GPUs)
  - FPGAs
  - Special function “chiplets” implemented as ASICs

- Increase network bandwidths
  - Within boxes and between boxes

- Promote IP architectures and standards
  - Efficient development of System-On-a-Chip (SOC) devices
  - “Software defined spacecraft” for small mission classes

- Use “managed COTS” (Commercial Off the Shelf) where appropriate
  - Understand radiation susceptibilities
  - Determine appropriate mission applications
  - Employ “layered” fault tolerance
  - Consider resource implications of fault tolerance scheme
Current Challenges

• How best to leverage HPSC in our hardware architectures
  – Optimal processing partition between processor elements within hybrid architectures
  – Signal integrity, EMI/EMC (Electromagnetic Interference / Electromagnetic Compatibility) and management of multiple (up to 24) high frequency (10GHz) interconnects
  – Providing multiple power services and ensuring power/ground quality
  – Adaptation of slice architecture to accommodate high speed networks

• How best to leverage HPSC in our software architectures
  – Adaptation of cFS to HPSC
  – Combination of mixed criticality applications in a complex multicore processing environment
  – Image/signal processing libraries ported to HPSC

• Technology needs
  – Intelligent, fault tolerant, multi-output Point-of-Load (POL) conversion
  – Advanced spaceflight memories
  – Next generation radiation tolerant FPGAs
  – “Special Function” chiplets with SRIO (Serial RapidIO) connectivity
  – Fault tolerant IP architectures, standards, and libraries
Current Challenges

- **Smallsat needs**
  - Smallsat subsystems and components with sufficient reliability and radiation tolerance for long duration missions in harsh environments
  - Standard onboard network interfaces

- **Use of COTS**
  - Growing reliance on COTS
  - Increasing complexity of COTS devices
  - Shortened product lifetimes
  - Reduced availability of radiation test facilities
  - Reliance on board-level or box-level radiation testing

- **Cybersecurity**
  - Increased attention within NASA
  - But no specific requirements have yet been levied on GSFC avionics

- **AI and deep learning in space**
  - Assessing potential onboard AI and deep learning applications
  - Defining the optimal flight architectures to implement them