A First Look at 22 nm FDSOI SRAM Single-Event Test Results

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Acronyms

- **22FDX®** – GlobalFoundries 22 nm Fully-Depleted SOI Process
- **BGA** – Ball Grid Array
- **DMEA** – Defense Microelectronics Activity
- **FD** – Fully Depleted
- **LET** – Linear Energy Transfer
- **LGA** – Land Grid Array
- **MBU** – Multi-Bit Upset
- **PD** – Partially Depleted
- **SOI** – Silicon-on-Insulator
- **SEFI** – Single-Event Functional Interrupt
- **SEE** – Single-Event Effect
- **SBU** – Single-Bit Upset
- **SRAM** – Static Random Access Memory
Introduction

• The per-bit cross-section for heavy ions was found to be identical in 65 nm and 45 nm partially depleted SOI SRAMs manufactured by IBM [Heidel TNS 2009]
  • However, the number of MBUs increased from 65 nm to 45 nm and only double bit errors were observed

• At 32 nm, direct-ionization proton effects were primarily studied, but there is some heavy ion data [Pellish TNS 2014]
  • No saturated cross-section was identified
  • Multi-bit upsets continue to increase and up to four bit upsets were observed
  • Little difference in roll angles was observed
Background

- RUFUS is a 128 Mbit SRAM test vehicle designed in GlobalFoundries 22 nm FDX process
  - FDX is fully-depleted SOI
- The nominal voltage is 0.8 V, but a range from 0.64 V to 1.08 V is supported by the technology
- Custom test boards were fabricated for single-event testing and interfaced to MicroZed™ for data collection and control
  - MicroZed™ is a low cost evaluation board that employs a Zynq® 7010
Part Preparation

• Samples were packaged in BGAs
• They were thinned to a minimum thickness of 80 μm
• After thinning, they were mounted on adapter boards that converted the BGA package to an LGA

Measured silicon thickness of test DUT
Image provided by DMEA
Test Conditions & Beams Used

- All voltages were nominal
- Static tests – write test pattern, irradiate, read back cells
- Dynamic tests – write memory block, read all cells in the block
  - This was repeated several times depending on the length of the irradiation

<table>
<thead>
<tr>
<th>Ion Species</th>
<th>Energy (MeV)</th>
<th>Nominal LET (MeV·cm²/mg)</th>
<th>Nominal Range (µm)</th>
<th>Tilt Angles (°)</th>
<th>Roll Angles (°)</th>
</tr>
</thead>
<tbody>
<tr>
<td>¹⁴N</td>
<td>195</td>
<td>1.3</td>
<td>379.6</td>
<td>0, 30, 45, 60, 62, 66, 71</td>
<td>0, 90</td>
</tr>
<tr>
<td>²⁰Ne</td>
<td>270</td>
<td>2.8</td>
<td>267.5</td>
<td>0, 30, 45, 60</td>
<td>0, 90</td>
</tr>
<tr>
<td>⁴⁰Ar</td>
<td>508</td>
<td>8.6</td>
<td>180.1</td>
<td>0, 30, 45, 60</td>
<td>0</td>
</tr>
<tr>
<td>⁶³Cu</td>
<td>729</td>
<td>20.3</td>
<td>123.5</td>
<td>0, 30, 45</td>
<td>0, 90</td>
</tr>
<tr>
<td>¹⁰⁹Ag</td>
<td>1170</td>
<td>43.6</td>
<td>107.2</td>
<td>0, 30</td>
<td>0</td>
</tr>
<tr>
<td>¹²⁹Xe</td>
<td>1366</td>
<td>53.1</td>
<td>107.7</td>
<td>0, 30</td>
<td>0, 90</td>
</tr>
</tbody>
</table>
Initial Results vs 32/45 nm

- Approximately an order of magnitude lower cross-section per bit in the 22 nm FDX® than was observed in either the 32 or 45 nm SRAMs
  - This is not surprising with the expected reduction in charge collection of fully-depleted SOI compared to partially depleted SOI
- The onset LETs, while not conclusively found, appear to be roughly the same for this node geometry
Cosine Law

- Appears to still follow cosine law
- Difference in cross-sections at same LET are about 30-50%
  - Increase with N may be due to high angles and increased MBU
  - Will continue to investigate with additional ions and with smaller angles
Input Pattern

No observable difference in the cross-sections as function of the input pattern (all 0s, all 1s, and logical checkerboard)
Single-Bit vs Multi-Bit Upsets

- Only single and double bit errors were observed
  - No higher order multi-bit upsets were observed
  - Angle did not increase likelihood of MBU
- The MBUs accounted for approximately 0.01% of the total number of errors
- At 45 nm, there was a strong dependence on input pattern with MBU probability, however, at 22 nm, all patterns were equally likely to exhibit MBUs
MBUs – Input Pattern

Pattern also does not appear to effect the likelihood of MBU
Roll Angle

- There is a strong directionality in the layout of the cells of the SRAMs and the transistors within the cells

- No apparent effect on the cross-section
No significant difference in 0° and 90° roll angle
Approximately 3-7% difference with the exception of copper at 45° tilt angle (~30%)
Copper at 45° may be due to ion range issues
Dynamic Testing – SEFI

• Dynamic testing wrote pattern to one block and then read the same block
  • Then moved to the next block and repeated until all 36 blocks had been written and read
  • This was repeated for the entire memory several times (12-30 depending on duration of the irradiation)

• Only one SEFI was observed: During the last Xe dynamic test, every address in one block was in error
  • This persisted through each subsequent R/W cycle until the irradiation concluded and was only cleared by a power cycle
  • Test conditions: All 1s pattern, LET = 53.1 MeV-cm²/mg, nominal supply voltages, average flux was ~500 cm⁻²/s
Initial Conclusions

• 22 nm FDSOI SRAM upset cross-section per bit is about an order of magnitude lower than 32 and 45 nm
  • Onset LETs appear to be similar, although additional testing is required to verify

• There does not appear to be any dependence on the roll angle or the input pattern, and cosine law is consistent with the tilt angle results

• MBUs accounted for a maximum of approximately 0.01% of the errors on any given run
  • Physical mapping of upsets is being attempted – MBU results may change substantially after post-processing

• One SEFI was observed when dynamically testing the DUT
  • Additional testing at higher LETs and with a laser will be conducted to investigate further
Future Work

• Additional single-event tests
  • More heavy ions
  • Laser test
  • Low-energy electrons
  • High-energy protons

• Investigate the effect of voltage on the SRAM array voltage (near threshold computing), as well as the n- and p-well voltages (body biasing)

• Further investigate the cosine law effect with additional low LET ions

• Further investigate SEFIs – cause and approximate likelihood

• Comparison to bulk 28 nm SRAM – process uses several of the same manufacturing steps as the 22 nm SOI
Acknowledgments

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