Implementation of Real-Time Hardware in the Loop Simulation for WAVE Instrument Avionics

Ali Al Qaraghuli
NASA Kennedy Space Center
Major: Electrical Engineering
NIFS Internship Program Falls Session
Date: 11/17/2017
Implementation of Real-Time Hardware in the Loop Simulation for WAVE Instrument Avionics

Ali Al Qaraghuli
NIFS INTERN, Kennedy Space Center, FL, 32899

The Regolith and Environment Science and Oxygen and Lunar Volatile Extraction (RESOLVE) payload will lead the Resource Prospector rover to hydrogen-rich locations on the moon supporting NASA’s in-situ resource utilization (ISRU) mission. The Water Analysis and Volatile Extraction (WAVE) system will be responsible for heating up regolith samples and analyzing their volatiles in a vaporized state. Given the space environment, testing flight hardware and software using the scientific instruments can be costly and time consuming, which can hold back progress involving the instruments. A hardware-in-the-loop (HITL) simulation will test the Avionics Data Acquisition as well as the Instrument Interface Unit, through simulating sensors and actuators involved in supporting the WAVE instruments. HITL is a platform for testing and developing WAVE’s avionics and software, where the simulation plant will imitate the LAVA and OVEN instruments, thus allowing for an accessible, efficient, and replicable testing environment.

Nomenclature

RESOLVE = Regolith and Environment Science and Oxygen and Lunar Volatiles Extraction
RP = Resource Prospector
LAVA = Lunar Advanced Volatile Analysis
OVEN = Oxygen Volatile Extraction Node
NIRVSS = Near Infrared Volatile Spectrometer Subsystem
NSS = Neutron Spectrometry Subsystem
WAVE = Water Analysis and Volatile Extraction
IIU = Instrument Interface Unit
HITL = Hardware in the Loop
ADAC = Avionics Data Acquisition
NE-L6 = Advanced Engineering Development Branch
GC = Gas Chromatography
MS = Mass Spectrometer
RTD = Resistance Temperature Detector
PT = Pressure Transducer
TEC = Thermoelectric Cooler
PWM = Pulse Width Modulation
NASA = National Aeronautics and Space Administration
DSN = Deep Space Network
ISRU = In-Situ Resource Utilization
PCB = Printed Circuit Board
DSUB = D-Subminiature
GND = Ground
VCC = Common Collector Voltage, Supply Voltage
KCL = Kirchhoff’s Current Law
LLS = Lunar Link Simulator
DDS = Software Message Bus
ENET = Ethernet
I. Introduction

The Advanced Engineering Development Directorate (NE-L6) at National Aeronautics and Space Administration (NASA) is designing, testing, and delivering hardware and software for Kennedy Space Center (KSC) research and technology projects for extraterrestrial In-Situ Resource Utilization (ISRU) on the lunar surface. Resource Prospector is NASA’s first moon-mining mission that aims to quantify water (and other volatiles) on the moon for future use. Given the cost of sending material into space, using the resources gathered on lunar environment will reduce the cost of launching infrastructure and resupply missions. The resources gathered will also be utilized to supply breathable oxygen and drinkable water along with rocket fuel for transport. The Resource Prospector mission will include various components, such as a lander, rover, payload, and launch vehicle. This paper will focus on the payload, known as RESOLVE (Regolith and Environment Science and Oxygen and Lunar Volatiles Extraction).

RESOLVE employs five major scientific instruments that will operate step-by-step in order to transform volatile-rich lunar regolith into analyzed volatiles. As the Rover tracks across the lunar surface, the Neutron Spectrometer Subsystem (NSS) will utilize Neutron Spectrometry to locate presence of Hydrogen. The presence of Hydrogen will give the team an indication of the presence of Water under the lunar surface. Once hydrogen is detected, the Drill Subsystem will dig into the surface and gather a sample of lunar regolith. As the Drill gathers regolith, the Near Infrared Volatile Spectrometer Subsystem (NIRVSS) will characterize the variability of the lunar surface and detect volatiles in soil extracted from the surface by the rover’s drill subsystem. Once categorized, the sample will be transferred into the 2-stage Water Analysis and Volatile Extraction (WAVE) instrument. The first stage is the Oxygen Volatile Extraction Node (OVEN) where the sample will be heated over 150°C, forcing it to enter a vaporized state. In the second stage of WAVE, the vaporized sample will be carried into the Lunar Advanced Volatile Analysis (LAVA) which will analyze the vaporized sample using Gas Chromatography and Mass Spectrometry. The data gathered would be processed by the payload’s computer, transferred to the rover’s computer, and then downlinked to the Deep Space Network (DSN) on Earth.

RESOLVE is a multi-center project. Different space centers will provide different scientific instruments, avionics, and software for the payload. The Kennedy Space Center responsibilities include the payload software development and payload avionics design for the LAVA and OVEN subsystems, coupled together as WAVE. This paper will focus on avionics and software integration testing for WAVE, and will discuss a testing strategy for the Avionics Data Acquisition (ADAC) and Instrument Interface Unit (IIU) by utilizing a real-time WAVE end item simulation.

II. Objectives

A. Goal

The goal of this project is to be able to simulate the WAVE instruments inputs and outputs, and be able to test the response of ADAC and IIU using a Hardware-in-the-loop simulation. HITL is a platform for development and testing of real-time embedded systems, often including complex simulation models and various interfaces. The WAVE instruments in this case are the “plant simulation”, represented by mathematical models that interface with
the embedded system through various analog and digital inputs and outputs. Replacing the WAVE instruments with mathematical models allows for advantages in cost, test flexibility, and safety. Given the tight schedule of the development and testing the WAVE instruments undergo, HITL allows for testing the simulation plant parallel to further development of the WAVE instruments. A major part of designing the HITL platform is simulating WAVE’s sensors and actuators into loads that mimic their actual behavior, and emulate their inputs and outputs. Some devices are easier to simulate than others, depending on the sensitivity of the measurement and range, a simulation of the sensors could be as simple as a resistor network, or as complex as an embedded system with multiple inputs and outputs. During the test, conditions can be manipulated and replicated until desired data is gathered.

B. Approach

Speedgoat and custom electronics will be emulating WAVE end items, such as temperatures and pressure measurements. The individual cards on the ADAC stack will respond to the real-time simulated inputs and outputs and act accordingly. For this phase of HITL development, LAVA measurements are selected. LAVA’s measurements are currently 48 RTDs, 36 heaters, 2 Marotta latching valves, 13 Mindrum latching valves, 3 piezoelectric valves, 1 TEC, and 7 PTs, in addition to power and communication busses. All devices and connections will be emulated during HITL.

The simulation plant will be running through Speedgoat. Speedgoat is a real-time target machine that contains various analog and digital input and output cards that will allow running complex physical models designed with MATLAB and Simulink. Speedgoat will be able to simulate a signal transmitted or received to and from each sensor/actuator using the digital and analog inputs and outputs. For example, LAVA RTDs during the mission will be reporting temperatures in the form of resistance and be read by the ADAC in the form of voltage, therefore Speedgoat will simulate the RTD’s temperature reading in the form of Analog Output into the Analog Measurement Card in the ADAC, which will be discussed in the avionics architecture.
C. Success Criteria

The test will be considered successful when ADAC and IIU acquire and process data from all sensors/actuators that are simulated given Speedgoat’s conditions. Another success criteria is the operation of all emulator circuits both individually and simultaneously. HITL will not be running under any environmental conditions (such as in thermal or vacuum chambers) for the purpose of this project, however, the test can be moved to be tested environmentally in the future.

D. Interfaces

HITL involves a large number of different networks and connections that carry different types of power and data. Connections are established between the IIU, ADAC, breakout boards, emulator circuit boards, and Speedgoat. The different cards on the ADAC will be communicating on the CAN bus through the backplane, and the IIU will communicate with ADAC as a whole over the CAN bus. Breakout circuit boards will be used to distribute the ADAC load connections into different channels that can connect to different simulated loads on the emulator circuits. The emulator circuits will connect to Speedgoat’s input or output channels based on the emulator load. In the case of a sensor, a single wire connection will be made from Speedgoat into the simulated load input. In the case of an actuator, a single wire will connect the simulated load’s output to Speedgoat’s digital or analog input. In any case where Speedgoat sends or receives a signal, a communication path takes place across all five components shown below in the diagram in either direction respectively.

E. Power

During the mission, Rover’s battery will supply 28V of unregulated power that can vary between 23V and 33V based on battery charge. During HITL, a power supply will emulate the power coming from the rover and going into the ADAC. IIU will be powered by ADAC. The Breakout and Emulator circuit boards require power aside from incoming and outgoing signals. Speedgoat will have its own power supply that can simply be plugged into an AC outlet.
F. Cables and Connectors

After identifying all of the HITL test setup connections, a cable plant connecting all the different items needs to be developed. This development includes building and integrating the cables, which is a multi-step process involving choosing proper gauge wires, stripping, crimping, and attaching connectors and adapters.

Another step is performing continuity checks on each wire between each connection. The ADAC cards will use Micro-D-subminiature connectors, while the connectors that interface with the ADAC cards are D-subminiature connectors. Most of the D-Sub connectors will be wired to the breakout printed circuit boards. Part of designing this test was designing circuit boards for any single ended device with a return line. A 50-pin breakout board, that splits into 25 channels, alongside a 25-pin connector, that has 12 channels, were designed and built for this test. The following figures display some of the PCB designs used in HITL test.
III. ADAC Architecture

The Avionics Data Acquisition (ADAC) is composed of a stack of printed circuit boards that perform various functions. The bottom of the stack is where the WAVE (LAVA and OVEN) avionics interfaces with the rover, and supply all the power going vertically up in the stack. Other cards in the stack include the Power Control Unit (PCU), the Power Distribution Unit (PDU), the Motor Control Card (MCC), the Analog Measurement Card (AMC), and finally the Top Cap. The ADAC stack communicates data with the Instrument Interface Unit (IIU), which stores the payload software. The separate cards will be communicating with each other and with the IIU through a back-plane array of connections which will employ CAN bus for communications as well as provide power to the cards from the PCU. Some cards exist in multiples since they employ a larger number of sensors and/or actuators. The function of the cards can be expressed in the following table:

<table>
<thead>
<tr>
<th>Card</th>
<th>Quantity</th>
<th>Function</th>
<th>User</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Cap</td>
<td>1</td>
<td>Power piezoelectric valves, thermoelectric cooler, CAN Bus, Mass Spectrometer Power</td>
<td>Shared by LAVA and OVEN</td>
</tr>
<tr>
<td>Analog Measurement Card</td>
<td>3</td>
<td>Measure analog values, mainly of RTD and PT sensors, reports values to other cards such as PDU</td>
<td>2 for LAVA, 1 for OVEN</td>
</tr>
<tr>
<td>Motor Control Card</td>
<td>2</td>
<td>Control motor channels and some heaters, resolvers, and potentiometers</td>
<td>OVEN only</td>
</tr>
<tr>
<td>Power Distribution Unit</td>
<td>3</td>
<td>Supplies power to heaters, latching valves, and proportional valves for LAVA, alongside Water Droplet Demo power and LEDs for the camera.</td>
<td>LAVA only</td>
</tr>
<tr>
<td>Power Control Unit</td>
<td>1</td>
<td>Provide power for other cards through the backplane, works with End cap to distribute rover power</td>
<td>Shared by LAVA and OVEN</td>
</tr>
<tr>
<td>End Cap</td>
<td>1</td>
<td>Provide analog and digital power, and CAN connections, connect to the rover</td>
<td>Shared by LAVA and OVEN</td>
</tr>
</tbody>
</table>

Table 1. ADAC Stack Breakdown

Figure 7. ADAC Full Stack (for LAVA and OVEN)
IV. Design Plan and Implementation

HITL employs various hardware and software components that run together real-time continuously. Based on the sensors/actuators needed in the test, different cards from the ADAC are used. For simulating temperature environments for RTDs or PTs, an AMC card needs to be connected in order to test ADAC’s ability to process the measurements. HITL must use all simulated sensors and actuators for LAVA, and eventually for OVEN, and then full stack (LAVA and OVEN).

A. RTD Simulation

In order to design the RTD emulator circuit, the driving circuit has to be taken into consideration in order to determine how the RTD can be simulated as a load. The following circuit shows the RTD (portrayed as “RTD1”) in connection with the AMC. Based on the resistance of the RTD, the voltage across the RTD line is amplified by the op-amp and directed towards an analog-to-digital converter through the “RTDOUT1” line. The amplified output is transferred to the PDU through the CAN bus, and the RTD measurements allow the Proportional, Integral, and Derivative (PID) control feedback loop to adjust the Pulse Width Modulation (PWM) duty cycle for signal going towards the heaters. Some RTDs are employed for temperature measurements (telemetry) only with no loop control.

![RTD Driver Circuit](image)

**Figure 8. RTD Driver Circuit**

From the circuit above, the RTD interfaces with the AMC and forms a divider network with the 15kΩ resistor.

B. Simulated Load Circuit Design

In order to design a circuit that simulates a sensor/actuator, the key is designing a load that responds to inputs and outputs the same way the sensor/actuator would. For example, in the case of the RTD, a measurement of temperature is based on the voltage measured across the variable resistor. Speedgoat would simulate the environment by outputting a voltage to the simulated load. From the RTD circuit above, given the high input impedance of the operational amplifier, the RTD divider circuit can be isolated the analysis can be performed for the following circuit:
A simulated RTD could take the form of a simple voltage divider, where the combination of R1 and R2 step down the standard 0-10V input voltage from Speedgoat to what the AMC would be expecting from the RTD based on certain temperature inputs. The circuit would look like the following:

By looking calculating the voltage divider values across the RTD circuit, it’s concluded that the AMC would expect a voltage of 0.1667V at -50°C, and 0.3463V at 200°C (C). Therefore the values of R1 and R2 have to be chosen such that their output voltage would give out 0.1667V at 0V input, and 0.3463V at 10V. By labelling I1 as the current going through R1, I2 as current running through R2, and I3 as current running from VCC through R3, the solution was found using Kirchhoff Current Law:

\[ i_1 - i_2 + i_3 = 0 \]

\[ \frac{V_{in}-V_o}{R_1} - \frac{V_o}{R_2} + \frac{V_{cc}-V_o}{R_3} = 0 \]

\[ \frac{V_{in}}{R_1} - \frac{V_o}{R_1} - \frac{V_o}{R_2} + \frac{V_{cc}}{R_3} - \frac{V_o}{R_3} = 0 \]

\[ V_o \ast \left( -\frac{1}{R_1} - \frac{1}{R_2} - \frac{1}{R_3} \right) = -\frac{V_{in}}{R_1} - \frac{V_{cc}}{R_3} \]

\[ V_o = \frac{V_{in} + V_{cc}}{\left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right)} \]
The equation above gives us a function where an output voltage can be calculated given an input voltage, supply voltage, and the resistor values. By assuming $V_{cc} = 3.3\text{V}$, $R_3 = 15\text{k}\Omega$, $V_{in} = 0\text{V}$ where $V_o = 0.1667$, and $V_{in} = 10\text{V}$ where $V_o = 0.3463$, we can set up two equations and solve for the unknown resistance values.

$$\frac{V_{in}-V_o}{R_1} + \frac{V_o}{R_2} + \frac{V_{cc}-V_o}{R_3} = 0$$

$$\frac{0-0.1667}{R_1} - \frac{0.1667}{R_2} + \frac{3.3-0.1667}{15k} = 0$$

$$\frac{10-0.3463}{R_1} - \frac{0.3463}{R_2} + \frac{3.3-0.3463}{15k} = 0$$

A solution is found where $R_1 = 42.184\text{k}\Omega$, and $R_2 = 813.4\Omega$

Though the theoretical values of $R_1$ and $R_2$ are not available in single resistors, $41.2\text{k}\Omega$ and $806\Omega$ were used for $R_1$ and $R_2$ respectively, and the input to output voltage table was adjusted accordingly. The following graph and table show the final design results:

![Simulated RTD Circuit with chosen R1 and R2 values](image)

![Table 2. RTD Temperature to Voltage Values](table)

Based on the table provided, a relationship between voltage and temperature is established for Speedgoat. A curve fit can be plotted in order to establish a 4th order equation that describes the trends between temperature and input voltage. This equation can be used in Speedgoat’s Simulink model to simulate any temperature between the ranges of $-53.1345^\circ\text{C}$ all the way to $201.847^\circ\text{C}$. 

NASA KSC – Internship Final Report
C. RTD Emulator Schematic

The result of the previous analysis leads to the following design. The schematic below shows Speadgoat Connections as “Connector 1” and “Connector 2”, while showing breakout board connections as “J1-J16”.

This configuration distributes 16 analog output connections from Speedgoat to the RTDs through the breakout board. Depending on the size of the resistors, connectors, and the printed circuit board, up to 32 RTD channels can fit on a single emulator circuit.

![Figure 12. RTD Emulator Schematic](image)

D. Integration

The final step to the test is installing all equipment, establishing all circuit connections, and configuring the mathematical models for the plant simulation. All hardware is gathered in one station and localized in order to be used in a small lab setting. Such setting allows for easy troubleshooting and quick modifications to both hardware and software. Other integrated activities will be performed such as channelization, checking equipment list, safe-to-mate testing, and other interface verifications. Given the large number of inputs and outputs involved, all inputs and outputs must be checked prior to testing in order to protect equipment/circuitry and to insure accurate test results.

V. Conclusion

HITL serves as an efficient platform to test hardware and software components of the RESOLVE payload, more specifically in this case, of the WAVE instruments. The approach used for this specific platform involves various connections to different units, and requires inputs and outputs from other units such as loads and scientific instruments. To save time and cost, emulator circuits are used in order to replace such loads and scientific instruments, since the primary focus of the platform is to test the avionics and software subsystems of the payload.

Emulator circuits were discussed in this paper in the example of the RTD emulator circuit, and a step-by-step process of designing and implementing the emulator circuit resulted in a simulated load that would interface with the ADAC stack in a precise manner and provide/receive accurate readings to and from Speedgoat.

Although the eventual goal of HITL is to test WAVE avionics and software fully, which would require full emulation of all sensors, actuators, and connections involved, the test was broken down in multiple-stages where the
paper focuses on the first stage of performing the test using LAVA only. This setting requires a half-stack configuration (2 AMCs, 3 PDUs, Top Cap, End Cap, and a PCU). Following the success of this half-stack configuration, the full-stack can be tested given that the design of all emulator circuits is complete.

A mock-up test of the RTD emulator circuit was conducted in order to test the established connection between ADAC and speedgoat. The output voltages measured were all within a 5% range of calculated output voltages. Some of the error is attributed to the use of 1% tolerance resistors for the divider network, alongside a 5% tolerance resistor for the supply resistor. The purpose of the initial RTD testing was to test the proof of concept rather than gather accurate measurements, since measurements can be enhanced by using low tolerance resistors such as 0.01% which would eliminate most of the error. A more accurate power supply can be used for more accurate results, which will take place in the future. Another source of error was the use of a curve fit for temperature to voltage establishment. The 4th order equation, \( y = -29.81x^4 + 486.91x^3 + 396.11x^2 + 1098.2x - 247.57 \), while moderately accurate, is not exact. This can be improved by using a higher order differential equation, or by compiling an array of linear interpolations between each point for more accurate conversion.

At the time that this paper is written, only the RTD circuit has been tested, and other sensors and actuators are under development and are planned to be tested before the end of the internship. The final goal is to have a HITL test involving the full WAVE avionics stack, simulating all sensors and actuators in both LAVA and OVEN.

Acknowledgments

This project would not have been completed without the intensive help of the WAVE Avionics and Software teams, who provided an exceptional learning environment in a professional atmosphere, without sacrificing the larger goal at hand. A special acknowledgment goes to Beau Lloyd Peacock, the mentor of this project, who provided guidance and support throughout the entire process. Recognition also goes to Curtis Ihlefeld, Christopher Forney, Christopher Reeves, Alex Decamargo, Christopher Bond, Steve Simmons, Rene Fermoso, Nathan Cain, and Josephine Santiago-Bond, who aided with this project and provided guidance through answering questions with detailed explanations.

References


