Getting SiC Power Devices Off the Ground: Design, Testing, and Overcoming Radiation Threats

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## Abbreviations & Acronyms

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<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
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<tbody>
<tr>
<td>GCR</td>
<td>Galactic Cosmic Ray</td>
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<tr>
<td>$I_D$</td>
<td>Drain Current</td>
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<tr>
<td>$I_G$</td>
<td>Gate Current</td>
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<tr>
<td>$I_R$</td>
<td>Reverse-Bias Leakage Current</td>
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<tr>
<td>ICSCRM</td>
<td>International Conference on Silicon Carbide and Related Materials</td>
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<tr>
<td>JFET</td>
<td>Junction Field Effect Transistor</td>
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<tr>
<td>LBNL</td>
<td>Lawrence Berkeley National Laboratory cyclotron facility</td>
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<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
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<tr>
<td>RHA</td>
<td>Radiation Hardness Assurance</td>
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<tr>
<td>RHBD</td>
<td>Radiation Hardened By Design</td>
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<tr>
<td>SEB</td>
<td>Single-Event Burnout</td>
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<thead>
<tr>
<th>Acronym</th>
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<tbody>
<tr>
<td>SEE</td>
<td>Single-Event Effect</td>
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<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>SiC</td>
<td>Silicon Carbide</td>
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<tr>
<td>SOA</td>
<td>Safe Operating Area</td>
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<tr>
<td>TAMU</td>
<td>Texas A&amp;M University cyclotron facility</td>
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<tr>
<td>TID</td>
<td>Total Ionizing Dose</td>
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<td>VDMOS</td>
<td>Vertical Double-diffused MOSFET</td>
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<tr>
<td>$V_{DS}$</td>
<td>Drain-Source Voltage</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate-Source Voltage</td>
</tr>
<tr>
<td>$V_R$</td>
<td>Blocking Voltage</td>
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Outline

• **Part 1: Design**
  – Understanding single-event effects susceptibility of SiC power devices through heavy-ion test data on different device types

• **Part 2: Testing**
  – Additional findings from heavy-ion test conditions

• **Part 3: Overcoming Radiation Threats**
  – Putting design insights into action: radiation hardening of a 1200 V SiC MOSFET
  – Radiation Hardness Assurance conclusions

Solar Electric Propulsion
image courtesy of NASA

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SEE radiation requirements are derived in part by the environment specified as a function of linear energy transfer (LET) in silicon; SiC test results therefore are in LET(Si)
PART 1: DESIGN
SINGLE EVENT EFFECTS: LEARNING FROM DIODE DESIGNS
Schottky Diode Effects: Degradation

Onset $V_R$ for degradation is similar for 650 V – 1700 V Schottky diodes: Electric field may not be a primary factor.

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Onset $V_R$ for degradation is higher for PIN diodes: The Schottky contact may contribute an additional mechanism.

Degradation:
- D1_650V
- D2_1200V
- D4_1700V
- PN5_1200V
- PN6_3300V

Increasing $I_R \propto$ ion fluence

No Measurable Effect

Increasing $I_R$ during irradiation

Degraded $I_R$ during irradiation

PIN Diodes

Reverse/Blocking Voltage

Q Collection

Measurement Results
Schottky Diode Effects: SEB

650 V – 1700 V Schottkys show SEB at similar fraction of rated $V_R$: Electric field dependent

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Schottky vs. PIN Diode Effects: SEB

SEB: sudden high-$I_R$ event
Increasing $I_R \propto$ ion fluence
Q Collection

Reverse/Blocking Voltage

Catastrophic Failure: Inability to block $V_R$
Degraded $I_R$
No Measurable Effect

During Irradiation
Post Run

Measurement Results

No difference between Schottky and PiN diodes for normalized SEB onset voltage

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SINGLE EVENT EFFECTS: LEARNING FROM JFET DESIGNS
JFET Effects as a Function of $V_{DS}$ at Fixed off $V_{GS}$: Degradation

Measurement Results

Degradation in normally-on and normally-off JFETs in this study is always drain-gate leakage, suggesting a trench design.
JFET Effects as a Function of $V_{DS}$ at Fixed off $V_{GS}$: Degradation

**Measurement Results**

- During Irradiation
  - Increasing $I_{DG}$
  - $I_D = I_G$
  - Q Collection
  - No Measurable Effect

- Post Run
  - Degraded leakage
  - $I_D$ & $I_G$

Columns: no effects

Error bars: Onset of degradation or SEB

**Onset $V_{DS}$ for degradation is similar for normally-on and (non-cascaded) normally–off JFETs**

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JFET Effects as a Function of $V_{DS}$ at Fixed off $V_{GS}$: Degradation

**Measurement Results**

1200 V & 1700 V JFETs have similar normalized onset $V_{DS}$: Greater field dependence of degradation mechanism vs. diodes (due to gate involvement or to lower LET?)

**Drain-Source Voltage**

- Increasing $I_{DG} \propto$ ion fluence:
  - $I_D = I_G$
  - Q Collection

- Degraded leakage
- No Measurable Effect

**Max passing $V_{DS}$**

Error bars: Onset of Degradation or SEB

**Graph**

- J1-J3 $V_{GS} = 0$ V: J4 $V_{GS} = -15$ V

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JFET Effects as a Function of $V_{DS}$ at Fixed off $V_{GS}$: SEB

SEB: sudden high-I event

Catastrophic Failure: $BVDSS \ll $ rated

Increasing $I_{DG}$

$\propto$ ion fluence:

$I_D = I_G$

Degraded $I_D$ & $I_G$

Q Collection

No Measurable Effect

During Irradiation

Post Run

Measurement Results

1200 V – 1700 V JFETs show SEB at similar fraction of rated $V_{DS}$

Normally-on similar to normally-off JFET susceptibility

Max $V_R$ no immediate SEB

Error bars: Onset of SEB

J4 $V_{GS} = -15$ V;
J1-J3 $V_{GS} = 0$ V

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SINGLE EVENT EFFECTS: LEARNING FROM MOSFET DESIGNS
MOSFET Effects as a Function of $V_{DS}$ at $V_{GS} = 0$ V: Latent Gate Damage

**Measurement Results**

- **No latent damage to gate from low LET/light ions;**
- **Onset is independent of MOSFET voltage rating at higher LETs**

**Graphical Data**
- Green = $V_{DS}$ range for which only latent damage occurs
- Grey = no ion effects

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MOSFET Effects as a Function of $V_{DS}$ at $V_{GS} = 0$ V: Degradation During Beam Run

Not all MOSFETs exhibit drain-gate leakage current degradation: Design techniques may eliminate this vulnerability

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MOSFET Effects as a Function of $V_{DS}$ at $V_{GS} = 0$ V: Degradation During Beam Run

$I_{DS}$ degradation least influenced by electric field and ion LET: linked to material properties??

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MOSFET Effects as a Function of $V_{DS}$ at $V_{GS} = 0$ V: SEB

- **SEB:** sudden high-$I$ event
  - $I_{DG}, I_{DS}$
  - $\Delta I_D >> \Delta I_G$
  - $I_{DG}$
  - $\Delta I_D = \Delta I_G$

- **Catastrophic Failure:**
  - $BV_{DSS} < 2$ V
  - $I_{DSS}$
  - or Failed $I_{GSS}$
  - $I_{GSS}, I_{DSS}$
  - Failed $I_{GSS}$

- **Q Collection**
  - No Measurable Effect

**Measurement Results**

- **Drain-Source Voltage**
- **Q Collection**

**SEB vulnerability at LET(Si) < 1 MeV-cm$^2$/mg**

Vulnerability saturates before the GCR flux “iron knee”

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Normalized Onset Voltage for Immediate SEB: Comparison of Device Types

Onset for SEB similar across device types: ~40% to 50% of rated V; Use of real breakdown voltage would strengthen similarity across devices of different ratings
Summary of Design Insights

• SEB susceptibility similar across all device types suggesting common mechanism
  – E-field dependent
  – Saturated onset at ~40% – 50% of rated voltage
• **Schottky contact increases susceptibility of $I_R$ degradation but not SEB**
• $I_R$ and $I_{DS}$ degradation in diodes & MOSFETs may be most linked to material properties
  – Minimal E-field dependence
  – Susceptibility saturates at low LETs ( < 10 MeV-cm²/mg)
• **JFET $I_{DG}$ degradation, however, shows field dependence**
  – No difference between normally-on and normally-off designs
• **MOSFET $I_{DG}$ degradation is design-dependent – expected to be easiest effect to eliminate**
  – Does not occur at low LETs / lighter ions
• **MOSFET latent gate damage susceptibility occurs in all designs at very low $V_{DS}$**
  – Onset by ~100 $V_{DS}$
  – Does not occur at low LETs / lighter ions
  – Expected to be the most difficult heavy-ion effect to eliminate
PART 2: TESTING
Test Challenge: Identification of SEB SOA

Degradation is non-Poisson process: Prior damage can impact effect of next ions. Threshold for SEB can be affected, preventing accurate identification of “SEB-safe” region of operation.


Saturation: Heat? or Degraded E-field?
Rate of leakage current degradation in 1200-V power MOSFET increases with increasing temperature. Because SiC dopants may not be fully ionized at room temperature, important to test at application temperature!
Testing: Angle Effects

- **Diode & MOSFET (in $\Delta I_D >> \Delta I_G$ regime):**
  - Strong angle effect
  - At given $V_R / V_{DS}$, no degradation at 45°
  - Matching vertical component of E-field has no impact: Cosine law not followed

- **MOSFET (in $\Delta I_D = \Delta I_G$ regime):**
  - Follows cosine law
  - Path length through gate likely dominates angle effect
    (Vertical field reduced with angle)

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Summary of Testing Insights

• We may not be able to reliably define the SEB safe-operating area
  – Appropriate test fluence may not be achievable before damage influences SEB susceptibility
  – No longer a true “single-event effect” due to effect of prior ion strikes
• Temperature influences rate of current degradation
  – Application temperature testing may be required
• Strong angle responses will help reduce on-orbit susceptibility
  – May also make rate calculations difficult
• Lighter ions/lower LETs will reveal nuances between designs
  – Responses saturate quickly
PART 3: OVERCOMING RADIATION THREATS
Radiation Hardness by Design: 1200 V MOSFET

- Reduced SEB susceptibility
  - Thicker epilayer
- Degradation of $I_{DG}$ eliminated
  - Drain neck width reduction
- Minimal change in onset of other degradation effects:
  - $\Delta I_D >> \Delta I_G$
  - latent gate damage

Continued research and development efforts are necessary to understand residual degradation mechanisms!
Summary & RHA Conclusions

• SEB safe operating area is difficult to reliably define
  – Susceptibility quickly saturates before the high-flux iron knee of the GCR spectrum
  • Mission orbit will have less influence on risk

• Application-specific temperature testing may be necessary
  – Dopants not fully ionized at room temperature
  – Effects of temperature on SEB susceptibility must be established

• Some degradation mechanisms may persist despite RHBD efforts
  – Impact on device long-term reliability must be established

• Radiation hardening comes with a cost
  – As with Si power MOSFETs, electrical performance will suffer from hardening techniques

• Lighter ion/lower LET tests will reveal nuances between designs and aid on-orbit degradation predictions
  – Responses are saturated at LETs dictated by typical mission destructive-SEE radiation requirements
  – LET should be specified in terms of LET(Si) but penetration range must be for SiC

• Characterization data should include identification of voltage conditions at which different effects occur
  – Richer dataset will include how susceptibility to these effects changes with ion species/LET