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Sixty Earth-Days Test of a Prototype Pt/HTCC Alumina Package in Simulated Venus Environment

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Abstract
This paper presents experimental results of a prototype high temperature co-fired ceramic (HTCC) package with Au/Pt metallization in a three-phase harsh environment test that culminated with 60-day demonstration in simulated Venus surface environment of 465 °C with corrosive atmosphere at 90 bar pressure. The prototype package is based on previously developed and reported HTCC package successfully tested with multiple analog and digital silicon carbide (SiC) high temperatures semiconductor integrated circuits (ICs) at NASA Glenn Research Center in 500 °C Earth air ambient for over ten thousands hours, and short-term tested at temperatures above 800 °C. The three-phase harsh environment test started with 48 hours in 465 °C Earth air, followed by 48 hours in 465 °C nitrogen at 90 bar pressure and 1400 hours in simulated Venus surface environment of 465 °C with corrosive atmosphere at 90 bar. Initial analytical results of the package materials and surfaces after exposure to Venus environment are discussed to assess the stability of the packaging materials in the tested environments. The test in simulated Venus environment was implemented in the NASA Glenn Extreme Environment Rig (GEER). The results of this study suggest that an effective encapsulation of areas of surface metallization and vicinities may help to improve electrical performance of a HTCC alumina packaging system in Venus environment.

Key words
High temperature, HTCC, packaging, SiC, Venus.

I. Introduction
The prolonged operation of semiconductor integrated circuits (ICs) and associated packaging and integration technologies for long-term exploration of the surface of Venus is challenging due to the high temperature (460 °C), high pressure (9.4 MPa) and chemically corrosive atmosphere of the planet [1]. After experimental investigation of high temperature dielectric properties of a selected high temperature co-fired ceramic (HTCC) alumina in a temperature range from room temperature to 550°C [2], a packaging material system composed of this HTCC alumina with co-fired platinum (Pt) metallization was proposed for high temperature harsh environment device packaging applications. A prototype ceramic package with 32-I/O (inputs/outputs) and a compatible circuit board based on this HTCC material system have been developed [3] and successfully tested with multiple analog and digital silicon carbide (SiC) high temperatures semiconductor ICs (developed at NASA Glenn Research Center) in 500°C Earth air ambient for over ten thousands hours [4a, 4b], and short-term tested at temperatures above 800°C [5]. In order to examine the possibility using this packaging material system for long term exploration of Venus surface with temperature of ~465 °C, and a corrosive atmosphere at ~ 90 bar pressure, an HTCC alumina packaging substrate with co-fired surface Pt metallization was previously tested with a SiC IC in simulated Venus atmospheric conditions for three Earth weeks [6].

This paper discusses further and more in-depth testing of a customized prototype HTCC package with Au/Pt metallization with prolonged Venus environment exposure. Prior to the test of the 60-day simulated Venus environment exposure (Phase 3), the package (and packaged SiC IC) was first subjected to ~48 hours in 460 °C Earth-air (Phase 1) followed by ~48 hours in 460 °C ~90 bar N_2 (Phase 2). The testing in simulated Venus environment and high temperature pressurized nitrogen was implemented in the NASA Glenn Extreme Environment Rig (GEER) [7]. Initial analytical results of materials of the package after exposure to Venus environment are presented and discussed to evaluate the stability of the packaging material system in Venus environment. The observed electrical behavior of the two packaged SiC integrated circuits will be reported in detail later [8], but it has been reported that both circuits tested successfully operated throughout the entire test duration including 60 days in Venus surface atmospheric conditions [9].

II. Experimental

A. Ceramic Package and Integration

The ceramic electronic package (and the packaged SiC IC) was electrically connected to the measuring instruments outside of the GEER chamber via a custom-constructed high temperature high pressure feedthrough with a stainless steel tube of outer diameter of ¾ inches [10]. In order to be integrated into the inner diameter, ~ 0.65 inches, of the stainless steel tube of this feedthrough, a 32-I/O HTCC alumina package, measured as 1.075 in. x 1.075 in. x 0.1 in. [2], with Pt metallization, was diced using a diamond saw into three parts. The center part resulting from dicing the HTCC package was removed and the two end parts, with eight usable bond pads each, were joined to form a smaller package (Fig. 1) using a high temperature thick-film glass material. Two such test packages were made for this test. One of two packages (designated "Package 5") was electrolysis-coated with a thin Au layer on exposed Pt metallization surfaces before dicing. The second package (designated "Package 4") was coated with thick-film Au on Pt metallization surfaces. The packages were reinforced with small ceramic alumina dies mounted on the backside of the package along the seam line for better mechanical integrity using the thick-film glass material. After the glass was cured at 850 °C, an alumina based adhesive [11] was applied between the ceramic dies over the seam line on the backside, and cured at final temperature stage at 371 °C for 2 hours. The completed package measures 1.075 in. x 0.5 in. x 0.1 in.. Eight gold (Au) wires with diameter of 10 mil were then attached to Pt metallization pads on the backside of the package using gold paste fired at 850 °C in air ambient, four wires are on each long-side of the package as shown in Fig. 1. Each Au wire was connected/attached to two neighboring backside pads. A SiC ÷2/÷4 clock integrated circuit die [4b]

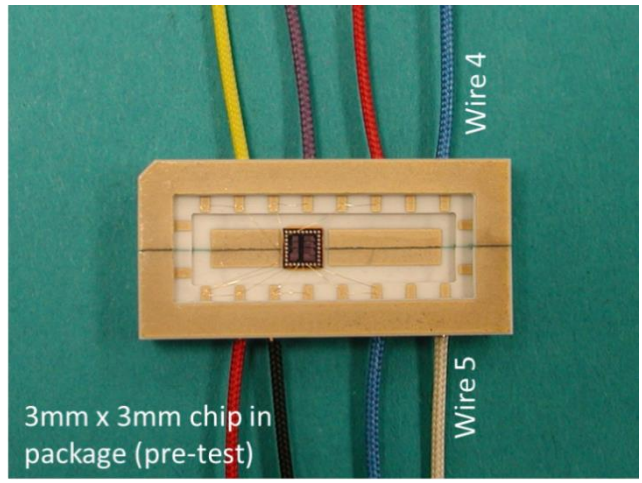

Figure 1: Package 5 with a SiC IC and two pads connected to Wire 4 and 5 for insulation test in simulated Venus environment. A thin Au layer was coated on co-fired Pt metallization surfaces. The color coded glass fiber sleeves were baked before integration with 20 mil Au wires extended from stainless steel tube.

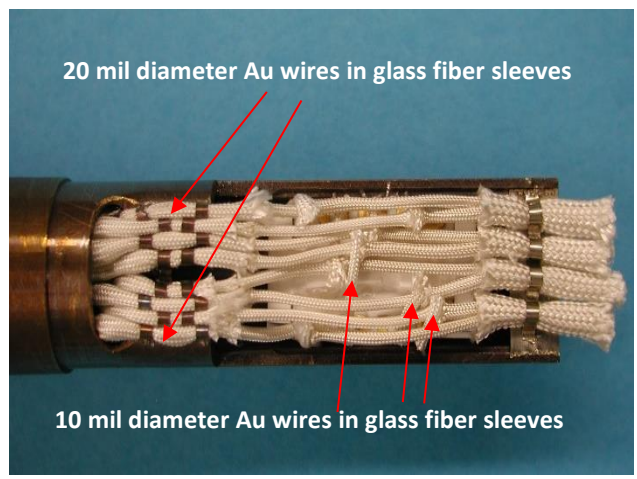

Figure 2: The picture of the inside-GEER end of test assembly 5 including package 5 with a SiC IC and insulation resistance measurement wiring for simulated Venus environment test. The packaged SiC IC shown in Fig. 1 was integrated into assembly 5, the package is underneath insulated wires and faces downward, the SiC IC is not visible in this picture.

was attached to each package using Au paste cured at 600 °C for two hours. One mil diameter Au wire-bonds (a few of which are barely visible in Fig. 1) connect the SiC IC to the package bond pads. The eight 10 mil Au wires were individually spark-welded to eight 20 mil diameter Au wires extending from the inside-GEER end of the stainless tube, as shown in Fig. 2, to the feedthrough (not shown). Six of these wires connected the SiC IC to the measuring instruments.

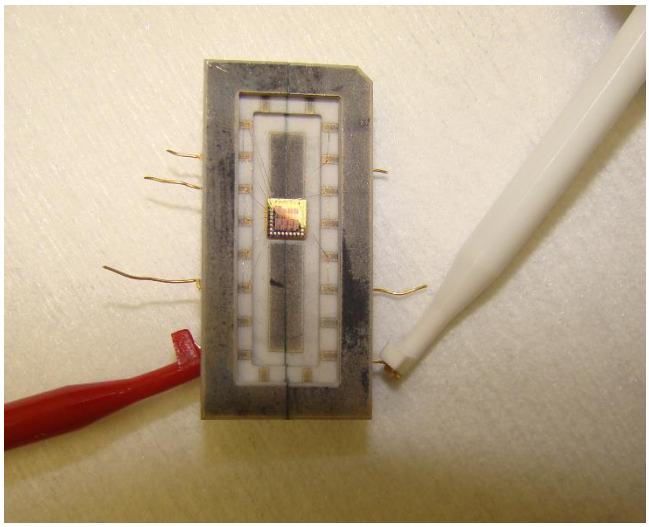

Figure 3: Package 5 with the SiC IC and Wire 4 and 5 for insulation resistance test after being disconnection from the 20 mil Au wires through stainless steel tube. The resistance between Wire 4 and 5 was measured directly by clipping Wire 4 and 5 to connect to SMU cable. The color of Au coated Pt metallization traces/pads changed significantly (compared with the picture in Fig. 1) after 60 days exposure to simulated Venus environment.

Two wires (designated "Wire 4" and "Wire 5", attached to separated package pads) were not connected to the SiC IC or each other, but were connected to two separate 20 mil diameter Au wires running through the stainless steel tube. These two wires were used for the purpose of monitoring of the electrical insulation resistance of the feedthrough in parallel with the package throughout the course of the three-phase harsh environment testing. Each 20 mil Au was individually insulated using fiber glass sleeves, shown in Fig. 2. The packages (packaged SiC ICs) were "facing down" in the stainless steel tube. The test was conducted without a lid, so both packages and SiC ICs were fully exposed to the testing environments.

B. Electrical Testing

In addition to the electrical testing of the packaged SiC ICs, DC insulation resistances between Wire 4 and Wire 5 of both test assemblies were measured to evaluate the parasitic leakage of the package and wiring system in all three phases of the environmental testing. The I - V curves between Wire 4 and 5 was measured via the other (outside-GEER) ends of 20 mil Au wires of the feed-through using a computer controlled Keithley 2400 source-measurement unit (SMU), the data was acquired with following SMU setting: The integration time of the SMU was set at 16.67 ms and time delay between two voltage steps was 0.1 s. The electrical resistance was calculated from the slope of the I-V curve below the compliance current limit setting of the SMU. Most

Table 1: The mixing ratios of gases used for simulated Venus environment in GEER [6].

Gas	Mixing (Mole) Ratio
CO_2	0.965
N_2	0.035
SO_2	18.0×10^{-5}
OCS	5.10×10^{-5}
H_2O	3.00×10^{-5}
CO	1.20×10^{-5}
H_2S	0.20×10^{-5}
HCl	5.00×10^{-7}
HF	2.50×10^{-9}

I-V curves were scanned between 0 to 50V, but in some cases the scanning voltage range had to be reduced to keep measured currents below SMU compliance current limits. The slope of best linear fit of the I-V curve (before the current reached the current limit of 1 mA compliance current limit set to the SMU) was used to extract the total resistance between Wire 4 and 5. Since the insulation resistance between Wire 4 and 5 of the package was measured at the other ends of the feed-through wires, so the measured resistance data includes the resistance between Wire 4 and 5 of the package in parallel with the insulation resistance between the two 20 mil diameter Au wires running through the stainless steel tube. Ideally, the electrical insulation resistance measured between Wire 4 and Wire 5 throughout testing should be an open circuit well above GΩ with low leakage or crosstalk of electrical signal between these two wires. The insulation resistance was first characterized throughout Earth air ambient from room temperature to 465 °C (Phase 1) before loading the test assemblies onto the Glenn Extreme Environment Rig (GEER), followed by Phase 2 in high pressure N_2 (GEER N_2), and Phase 3 in simulated Venus surface environment in GEER. The measurements of insulation resistance were also performed during upward and downward temperature ramps.

C. GEER Operation

The GEER chamber is a 3 ft diameter and 4 ft long cylindrical stainless steel pressure vessel designed for long duration testing in extreme conditions. The simulated environment is achieved with a fully automated high pressure gas delivery system, multicomponent gas mixer, and high pressure gas pump. The chamber is uniformly heated by internal electric heaters that are controlled by the facility programmable logic controller (PLC). This test in GEER included two test phases (Phase 2 and 3), a brief test

cycle (Phase 2) with nitrogen followed by a 60 day test with the simulated Venus gas mixture (Phase 3) [6]. The GEER chamber was first purged with dry nitrogen gas and evacuated to 0.1 bar to reduce gas impurities. The vessel was then filled to 36.5 bar at ambient temperature with pure nitrogen, and heated at 7 °C/hour to the target conditions of 460°C temperature and 92 bar pressure. The conditions were held for 48 hours before transitioning to Phase 3 with the simulated Venus environment. Prior to filling with the simulated Venus gas mixture, the vessel temperature was reduced to 150°C and then depressurized to 1 bar. Next, Venus simulating gas mix was then automatically filled in the quantities needed to achieve the mixing ratios listed in Table 1. Vessel temperature was held at 150°C during the filling process. Once all constituents were delivered to the vessel, the simulated Venus gas mixture was heated at 7 °C/hr until reaching the target test conditions of 92 bar at 460 ± 5 °C. The test in simulated Venus environment lasted 60 Earth days during which the gas mixture was periodically sampled and adjusted to the targeted mix ratios. The gas mix of simulated Venus environment is shown in Table 1 [6].

D. Surface Analysis and FIB

After the test in GEER, ceramic package 5 was examined by x-ray photoelectron spectroscopy (XPS), focused ion beam (FIB) cross-section milling and field-emission scanning electron microscopy (FE-SEM)/energy dispersive x-ray spectroscopy (EDS) to study the durability of the package materials as well as surface conditions after long term exposure to the simulated Venus surface environment. XPS analysis was performed on a PHI 5000 Versaprobe using monochromatic microfocused Al x-rays (43.4 W) with a photoelectron takeoff angle of 45° and 200 µm diameter area of analysis. The FE-SEM imaging and FIB cross section milling were carried out in a FEI Helios NanoLab™ 650 Ga dual beam FIB equipped with an Oxford Instruments 80mm^2 XEDS Silicon Drift Detector (SDD) system. A thin Pt layer was deposited on the analysis area to protect the cross section during milling. A Focused Ga beam of 30keV was used for milling, and 2keV e^- beam was used for FE-SEM and EDS data acquisition.

III. Results and Discussion

A. Insulation Resistance

It is an open circuit between Wire 4 and Wire 5, so ideally the resistance between Wire 4 and Wire 5 should be very high and independent of temperature and time. However, the insulation resistances of both assemblies measured during all 3 phases of testing changed substantially with temperature and testing time.

Fig. 4 shows the measured insulation resistances between Wire 4 and Wire 5 of assembly 4 and assembly 5 as functions

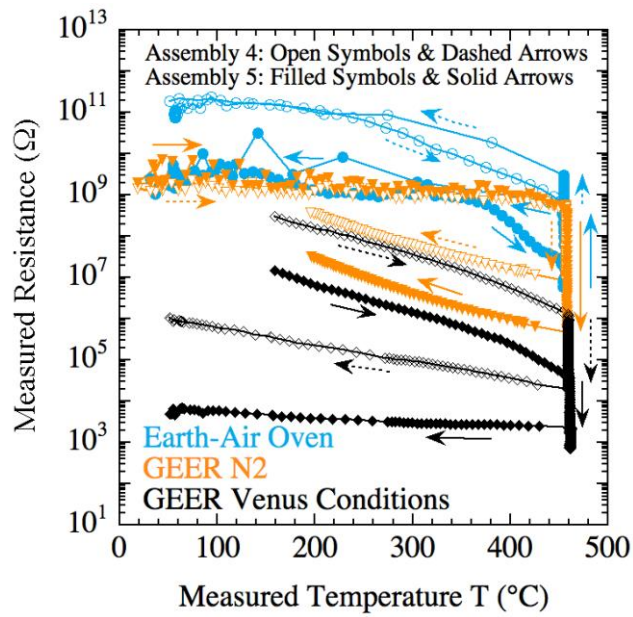

Figure 4: The insulation resistance data between Wire 4 and 5 of package 4 and 5 measured as functions of temperature in air ambient, GEER nitrogen, and GEER Venus conditions. The vertical data points at 460±5 °C are plotted as functions of time in Fig. 5.

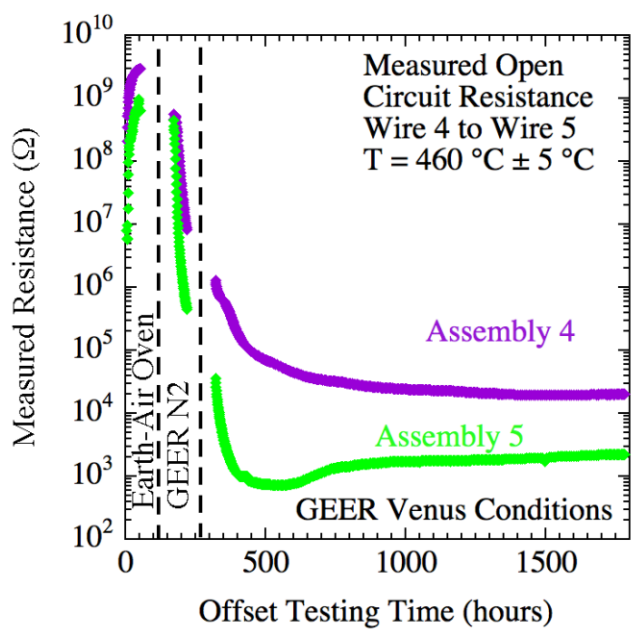

Figure 5: The insulation resistance data between Wire 4 and 5 of package 4 and 5 measured in 460 ±5 °C in air ambient, GEER nitrogen (90Bar pressure), and simulated Venus environment. The time axis shows the total test time, the temperature in the periods with data points shown is 460 ±5 °C. During the transition periods the chamber temperature is lower.

of temperature in Earth air ambient, GEER nitrogen, and GEER Venus conditions. The data chart presents the temperature dependent resistances of both assemblies during the upward temperature ramp toward 460 ± 5 °C, constant temperature dwell at 460 ± 5 °C, and downward ramp towards room temperature of all three phases of Earth Oven, GEER N_2, and GEER Venus conditions. The resistances of both assemblies decrease significantly with temperature increase for all the temperature ramps. The temperature dependence of resistances are approximately reversible in Earth air, but the changes of resistances in GEER N_2 and GEER Venus conditions are largely not reversible. It is noteworthy that in Earth air phase the pressure is constantly 1 atm, but the pressure in GEER N_2 increases with temperature and reaches 90 bar when the temperature reaches 460 ± 5 °C. The insulation resistances of both assemblies decrease severely in Phase 3 GEER Venus conditions, and are not reversible. The total drops of insulation resistances, after three-phase test, are over five orders of magnitude.

The insulation resistances decrease at 460±5 °C with testing time. Fig. 5 shows the measured insulation resistances between Wires 4 and 5 of assembly 4 (blue) and assembly 5 (green) vs. time with the package at 460 ± 5 °C ambient temperature during all 3 testing phases. As shown in Fig. 5, for the first testing phase in 460 ± 5 °C Earth-air, the insulation resistance of assembly 5 with package 5 is initially 7.9 MΩ and increases to 650 MΩ after 48 hours at this temperature, while the assembly 4 insulation resistance is initially at 210 MΩ and increases to 3.0 GΩ.

In the second phase test in GEER N_2 at 90 bar, the insulation resistances vary with time at 460 ± 5 °C negatively, exhibiting substantial degradation. In particular, the resistance of assembly 5 starts at 384 MΩ and sharply decreases almost 3 orders of magnitude to 448 kΩ at 48 hours in GEER N_2 at 90 bar as shown in Fig. 5, while the insulation resistance of assembly 4 similarly decreases from 424 MΩ to 7.6MΩ. Since N_2 is generally regarded as a mostly inert gas, the large degree of insulation resistance degradation over the time at 460 ± 5 °C was unanticipated.

In phase 3, GEER Venus conditions, the measured assembly insulation resistances continue the downward trend. As shown in Fig. 5, the resistance of Assembly 5 is 45kΩ in 460 ± 5 °C GEER Venus condition initially, and further decreases to 721 Ω as the minimum measured resistance at 231 hours, before gradually increases to 2.26 kΩ at 1459 hours (~ 60 days) in GEER Venus condition, while the resistance of assembly 4 declines from 1.18 MΩ to 19.8k Ω in GEER Venus conditions.

After the final GEER test phase, the assembly 5 was removed from GEER for post-test disassembly and investigation to uncover the physical mechanism of the measured severe degradation of "open circuit" insulation resistance. Towards this end, a series of SMU I-V curves of assembly 5 curves were measured as assembly 5 was systematically taken apart. Prior to the disassembly, the room-temperature insulation resistance between Wire 4 and Wire 5 of assembly 5 terminals was measured to be 12 kΩ.

The critical configuration for post-GEER-test diagnostic I-V measurement is depicted by Fig. 3, the resistance between Wire 4 and Wire 5 of ceramic package 5 was measured following its disconnection (i.e., physical and electrical isolation) from the rest of assembly 5. The ceramic package resistance between Wire 4 and Wire 5 measured at room temperature by directly clipping the 10 mil diameter Au wires as depicted in Fig. 3 was 21.7 MΩ. Meanwhile, the resistance measured between the corresponding long fiberglass-insulated 20 mil diameter Au wires running through the stainless steel tube and pressure seals (now entirely disconnected from the ceramic package 5 leads) was only 12 kΩ.

While the results of above measurements clearly exclude the HTCC ceramic package as the primary source of observed "open-circuit" insulation resistance degradation, the insulation resistance of 21.7 MΩ post-GEER-test package 5 Wire 4 to Wire 5 at room temperature is nevertheless substantially and permanently degraded too. Therefore, materials analysis described in the following section was conducted to see if physical evidences responsible for degraded insulation resistance could be observed.

B. Surface Analysis

Fig. 6 shows the EDS elemental map of a bond pad and the surrounding HTCC alumina surface. The yellow, green, and blue colors indicate distributions of Pt, S, and Al. In the area of box 16 of bond pad, as labeled in the Fig. 6, weight percentage of Pt, Au, S, and Al measured by EDS (C, O, and Al are also in EDS spectrum) are 47.1%, 36.4%, 9.4%, and 1.1%, respectively. EDS of a cross section of the bond pad generated by FIB (not shown) indicate that a thin non-uniformed surface layer of PtS resulted from reaction between the Pt bond pad and the sulfur containing gases in the simulated Venus environment, but the underlying Pt is not reacted. In box 23 of the alumina surface close to the Pt pad, weight percentage of Pt, S, C, and Al (O, Si, and Mg are also shown in EDS spectrum) are 1.2%, 0.5%, 1.9%, and 53.4%, respectively. Fig. 7 shows FE-SEM micrograph of alumina surface of ~ 45 µm x 25 µm on the left side of the bond pad shown in Fig. 6. Scattered particles of PtS, and alkaline earth impurities from the alumina are shown in Fig. 7. EDS elemental map (not shown) of Pt, Au, and S of the Pt bond pad shows that the distribution of Au originally coated on the top surfaces of the Pt pads, is no longer uniform and continuous.

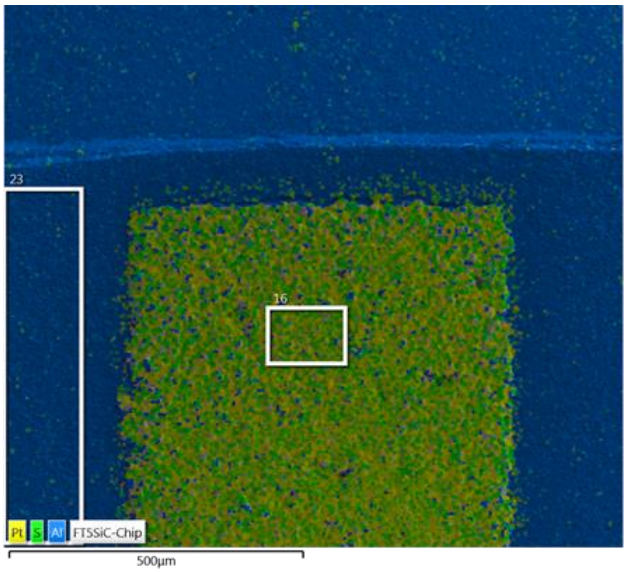

Figure 6: EDS elemental map of a bond pad and HTCC alumina regions surrounding the pad. The yellow, green, and blue dots indicate Pt, S, and Al distributions on bond pad and surrounding alumina surfaces.

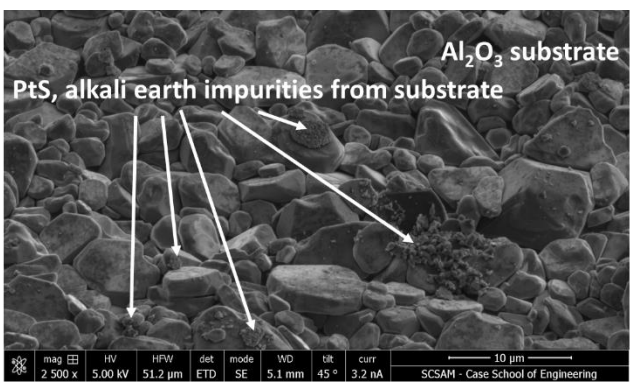

Figure 7: FE-SEM micrograph of alumina surface on the left side of the bond pad showing particles including PtS.

XPS of the exposed co-fired alumina surface of package 5 shows the presence of C, S, F, Na, Mg, Ca, Si, Fe, and trace amounts of Pt, in addition to the O and Al. The relative atomic surface concentrations of these elements before surface sputtering are shown in Table 2. After a 1 min. Ar^+ surface sputtering, the surface carbon is significantly reduced and Ca is eliminated. Relative atomic concentrations of remaining elements are shown in Table 2.

The FE-SEM and EDS results of the Pt pads show that even though a thin surface layer of PtS formed on the bond pads, underlying Pt remained chemically stable. Due to the reaction on the top surface of the bond pad the Au coating layer largely diffused and distributed non-uniformly. The surface color of the bond pads also changed from golden to grey as shown in Fig. 1 and 3. If these surface reaction and surface phenomena are strictly contained on bond pad surfaces, they may not have direct and significant impact on the electrical performance and packaging reliability. The mechanism of formation of the PtS/Pt particles on alumina surface near bond pads still needs to be investigated. It is unlikely that these scattered and isolated PtS/Pt particles significantly affect the insulation resistance of the package.
The results of the XPS study of the HTCC alumina surface indicate that while the alumina is stable in the simulated Venus environment, but its surface was contaminated by carbon and ionic compounds that may elevate surface conductivity, especially at high temperature.

IV. Summary and Conclusion

Two customer test packages based on previously developed HTCC alumina package with Pt metallization have been tested in simulated Venus environment for 60 Earth days. The bulk material system composed of co-fired Pt and 92% alumina has been shown to be chemically stable in long term Venus environment. The formation of a thin top surface layer of PtS was observed on originally Au coated Pt bond pads. Both packages successfully facilitated the test of SiC ICs in the simulated Venus environment, but the package electrical insulation resistance substantially degraded possibly caused by surface contaminations resulting from reactions of the impurities in alumina with Venus gases at high temperature and high pressure, and possible surface depositions from the simulated Venus environment. Surface encapsulation to protect metallization and alumina surfaces is suggested to further improve electrical performance and long term reliability of the HTCC packaging system for possible long term Venus surface applications.

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Table 2: Relative atomic concentrations of elements measured by XPS on alumina surface before and after Ar^+ sputtering.

Elements	C	Pt	Na	Mg	Ca	Fe	Si	S	F	O	Al
Prior sputtering	33.5	0	0.9	0.2	0.3	0.5	5.6	2.7	0.5	38.6	17.2
1 min. sputtering	7	0.2	0.3	0.3	0	0.9	1.9	1.2	0.3	57.9	30

References

[1] G.W. Hunter, "High Temperature Sensors and Electronics for Venus Missions," 6th International Planetary Probe Workshop, Atlanta, Georgia Short Course on Extreme Environments Technologies 06/21-22 2008.

[2] L. Chen, "Electrical Performance of Co-fired Alumina Substrates at High Temperatures," Journal of Microelectronics and Electronic Packaging (2013) 10, 89-94.

[3] L. Chen, P.G. Neudeck, D.J. Spry, G.M. Beheim, and G.W Hunter, "Electrical Performance of a 32-I/O HTCC Alumina Package for High-Temperature Microelectronics," Journal of Microelectronics and Electronic Packaging (2017) 14, 11-16.

[4a] D.J. Spry, P.G Neudeck, L. Chen, D. Lukco, C.W. Chang, G.M. Beheim, M.J. Krasowski, & N.F. Prokop, "Processing and Characterization of Thousand-hour 500 °C Durable 4H-SiC JFET Integrated Circuits," In Proceedings of iMAPS Int. Conf. High Temperature Electronics – HiTEC 2016, pp. 249-256. doi: 10.4071/2016-HITEC-249.

[4b] P.G. Neudeck, D.J. Spry, M. Krasowski, N.F. Prokop, L. Chen, and C. Chang, "Yearlong 500 °C Operational Demonstration of Up-scaled 4H-SiC JFET Integrated Circuits," in Proceedings of 2018 iMAPS HiTEC, Albuquerque, NM, May 8 – 10, 2018.

[5] P.G. Neudeck, D.J. Spry, L. Chen, N.F. Prokop, & M.J. Krasowski, "Demonstration of 4H-SiC Digital Integrated Circuits above 800 °C," IEEE Electron Device Letters, Vol. 38 Issue 8, 2017.

[6] P.G. Neudeck, R.D. Meredith, L. Chen, D.J. Spry, L. Nakley, & G.W. Hunter, "Prolonged Silicon Carbide Integrated Circuit Operation in Venus Surface Atmospheric conditions," AIP Advances 6, 125119 (2016); https://doi.org/10.1063/1.4973429.

[7] https://geer.grc.nasa.gov/

[8] P.G. Neudeck *et al*, to be published.

[9] Paul Vooson, Armed with tough computer chips, scientists are ready to return to the hell of Venus, Science News, November 2017: http://www.sciencemag.org/news/2017/11/armed-tough-computer-chips-scientists-are-ready-return-hell-venus

[10] To be published.

[11] https://www.aremco.com/news-item/ceramabond%E2%84%A2-503-now-used-to-bond-aluminum-oxide-ceramics/