SpaceCube: A Family Of Reconfigurable Hybrid On-Board Science Data Processors

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Background
The Challenge

The next generation of NASA science and exploration missions will require “order of magnitude” improvements in on-board computing power ...

Mission Enabling Science Algorithms & Applications

- Autonomous Operations
- Real-time Event / Feature Detection
- Real-time Sensing and Control
- On-Board Data Volume Reduction
- Real-time Image Processing
- On-Board Product Generation
- On-Board Classification
- Real-time “Situational Awareness”
- “Intelligent Instrument” Data Selection / Compression
- Real-time Calibration / Correction
- Inter-platform Collaboration
- Distributed Measurement Missions
Our Approach

- The traditional path of developing radiation hardened flight processor will not work ... they are always one or two generations behind
- Use the latest radiation-tolerant* processing elements to achieve 10x to 100x improvement in “MIPS/watt” (for the same size/weight/power)
- Accept that radiation induced upsets may happen occasionally and just deal with them appropriately ... any level of reliability can be achieved via smart system design

*Radiation tolerant – susceptible to radiation induced upsets (bit flips) but not radiation induced destructive failures (latch-up)
**Our Solution**

*SpaceCube: a high performance reconfigurable science / mission data processor based on Xilinx Virtex FPGAs*

- Hybrid processing ... CPU, DSP and FPGA logic
- Integrated “radiation upset mitigation” techniques
- SpaceCube “core software” infrastructure (cFE/cFS and “SpaceCube Linux”, with Xenomai)
- Small “critical function” manager/watchdog
- Standard high-speed (multi-Gbps) interfaces

*Note: SpaceCube 2.0 and SpaceCube Mini can be populated with either commercial Virtex 5 FX130T parts or radiation hardened Virtex 5 QV parts ... offering system developers the option of trading computing performance for radiation performance*
Being Reconfigurable …

... equals BIG SAVINGS (both time and money)

During mission development and testing
  • Design changes without PCB changes
  • “Late” fixes without breaking integration

During mission operations
  • On-orbit hybrid algorithm updates
  • Adaptive processing modes
    - hi-reliability vs. high-performance
    - intelligently adapt to current environment

From mission to mission
  • Same avionics reconfigured for new mission
Commercial Processor Trend

- Intel Core i7 3960X (Hex core)
- Intel Core i7 980 (Hex core)
- Intel Core i7 920 (Quad core)
- Intel Core 2 QX9770 (Quad core)
- AMD Athlon FX
- Intel Pentium 4
- AMD Athlon XP
- Intel Pentium III
- PowerPC 750
- Intel Pentium Pro
- Intel Pentium
- Motorola 68040

“Fastest” consumer CPU in 2011
Processor Trend Comparison

Intel Core i7 3960X (Hex core)
Intel Core i7 980 (Hex core)
Intel Core i7 920 (Quad core)
Intel Core 2 QX9770 (Quad core)
Intel Core 2 (Quad core)
AMD Athlon FX
AMD Athlon XP
Intel Pentium 4
Intel Pentium III
PowerPC 750
Intel Pentium Pro
Intel Pentium
Galileo
HST
ISS
EOS Terra
Mars Rovers
MRO
New Horizons
DAWN
LRO
SDO
Curiosity

Processor Trend Comparison - NASA Goddard Space Flight Center – November 2018
SpaceCube Closes the Gap

Next Generation Mission Processing Requirements (STMD, Decadal Surveys)

SpaceCube v1.0
SpaceCube v2.0

Commercial Processor Trend

Space Processor Trend

1,000x Gap

SCS750
RAD750
RAD6000
386
1750A
RCA 1802


2,600,000,000
2,000,000,000
1,000,000,000

100,000,000
10,000,000
1,000,000

2,300
10,000
20,000
100,000
1,000,000
10,000,000
20,000,000
100,000,000
2,000,000,000

## Processor Comparison

<table>
<thead>
<tr>
<th>Processor</th>
<th>MIPS</th>
<th>Power</th>
<th>MIPS/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIL-STD-1750A</td>
<td>3</td>
<td>15W</td>
<td>0.2</td>
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<tr>
<td>RAD6000</td>
<td>35</td>
<td>15W</td>
<td>2.33</td>
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<tr>
<td>RAD750</td>
<td>300</td>
<td>15W</td>
<td>20</td>
</tr>
<tr>
<td>LEON 3FT</td>
<td>75</td>
<td>5W</td>
<td>15</td>
</tr>
<tr>
<td>LEON3FT Dual-Core</td>
<td>250</td>
<td>10W</td>
<td>25</td>
</tr>
<tr>
<td>BRE440 (PPC)</td>
<td>230</td>
<td>5W</td>
<td>46</td>
</tr>
<tr>
<td>Maxwell SCS750</td>
<td>1200</td>
<td>25W</td>
<td>48</td>
</tr>
<tr>
<td>SpaceCube 1.0</td>
<td>3000</td>
<td>7.5W</td>
<td>400</td>
</tr>
<tr>
<td>SpaceCube 2.0</td>
<td>6000</td>
<td>10W</td>
<td>600</td>
</tr>
<tr>
<td>SpaceCube Mini</td>
<td>3000</td>
<td>5W</td>
<td>600</td>
</tr>
</tbody>
</table>
SpaceCube 1.0 vs RAD750

25 RAD750 6U Processor Cards

- Power: 600W
- Weight: 100-lbs
- Volume: 48.6 cu-ft

1 SpaceCube Processor Card

- Single String Box
  - Power: 600W
  - Weight: 100-lbs
  - Volume: 48.6 cu-ft

- Dual Redundant Box
  - Power: 37W
  - Weight: 7.5-lbs
  - Volume: 1.2 cu-ft
SpaceCube 2.0 vs SCS750 (per NSF CHREC)

Board Comparison

<table>
<thead>
<tr>
<th>Processor</th>
<th>CD (GOPS)</th>
<th>CD/W (GOPS/W)</th>
<th>EMB (GB/s)</th>
<th>IOB (GB/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SpaceCube v2.0 Processor Card</td>
<td>1007.44, 429.14, 119.34, 103.86, 29.92</td>
<td>44.3, 22.62, 5.91, 5.14, 1.7</td>
<td>32, 218.32</td>
<td></td>
</tr>
<tr>
<td>SCS 750</td>
<td>12, 6.4, 3.2, 1.6, 0.8</td>
<td>0.44, 0.22, 0.11, 0.05, 0.03</td>
<td>6.4, 6.4</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
- Power for PowerPC 750fx is ~9.7 Watts max. However, for 3x PowerPC 750fx processors it’s 29.1 Watts. No performance gain, but triple the power consumption lowers CD/W.
- Computational Density doubled for SpaceCube v2.0 (2x Xilinx FPGAs)
### Performance Comparisons

#### Computational Density (CD) & CD per Watt

<table>
<thead>
<tr>
<th>Processor</th>
<th>CD (GOPS)</th>
<th>CD/W (GOPS/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Int8</td>
<td>Int16</td>
</tr>
<tr>
<td>Honeywell HXRHPPC</td>
<td>0.08</td>
<td>0.08</td>
</tr>
<tr>
<td>BAE Systems RAD750</td>
<td>0.27</td>
<td>0.27</td>
</tr>
<tr>
<td>Cobham GR712RC</td>
<td>0.08</td>
<td>0.08</td>
</tr>
<tr>
<td>Cobham GR740</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>BAE Systems RAD5545</td>
<td>3.73</td>
<td>3.73</td>
</tr>
<tr>
<td>Boeing Maestro</td>
<td>11.99</td>
<td>11.32</td>
</tr>
<tr>
<td>Ramon Chips RC64</td>
<td>102.40</td>
<td>102.40</td>
</tr>
<tr>
<td>BAE Systems RADSPEED</td>
<td>14.17</td>
<td>11.81</td>
</tr>
<tr>
<td>Xilinx Virtex-5QV FX130</td>
<td>503.72</td>
<td>214.57</td>
</tr>
<tr>
<td>Xilinx Zynq-7020</td>
<td>283.3</td>
<td>152</td>
</tr>
</tbody>
</table>

**Notes:**
- **SPFP** = Single-Precision Floating Point
- **DPFP** = Double-Precision Floating Point
- Results assume an operations mix of 50% additions and 50% multiplications
Applications
## Algorithm Acceleration

<table>
<thead>
<tr>
<th>Application</th>
<th>Xilinx Device</th>
<th>Acceleration vs CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAR Altimeter</td>
<td>Virtex-4 FX60</td>
<td>79x vs PowerPC 405 (250MHz, 300 MIPS)</td>
</tr>
<tr>
<td>RNS GNFIR FPU, Edge</td>
<td>Virtex-4 FX60</td>
<td>25x vs PowerPC 405 (250MHz, 300 MIPS)</td>
</tr>
<tr>
<td>HHT EMD, Spline</td>
<td>Virtex-1 2000</td>
<td>3x vs Xeon Dual-Core (2.4GHz, 3000 MIPS)</td>
</tr>
<tr>
<td>Hyperspectral Data Compression</td>
<td>Virtex-1 1000</td>
<td>2x vs Xeon Dual-Core (2.4GHz, 3000 MIPS)</td>
</tr>
<tr>
<td>GOES-8 Ground System Sun correction</td>
<td>Virtex-1 300E</td>
<td>6x vs Xeon Dual-Core (2.4GHz, 3000 MIPS)</td>
</tr>
</tbody>
</table>

- All functions involve processing large data sets (1MB+)
- All timing includes moving data to/from FPGA
- **SpaceCube 2.0 is 4x to 20x more capable than these earlier systems**
On-Board Data Reduction

Accomplishments

SAR Nadir Altimetry Results (FY07)

On-board processing yields lossless 6:1 data volume reduction
On-Board Data Reduction (cont.)

Accomplishments

On-board product generation yields factor of 165x data volume reduction

SAR Mapping Results (FY09)

SpaceCube Output

Difference < 1%
On-Board Product Generation

• Classification
• Product Generation
• Event Detection
• Atmospheric Correction
Robotic Satellite Servicing

- Autonomous rendezvous & docking
- Robotic servicing

- Inspect
- Refuel
- Repair
- Replace
- Relocate
Imaging Spectrometers

- Direct broadcast
- Real-time products
- Data volume reduction
- Adaptive processing
- Sensor webs

Image Credit: HyspIRI Mission Concept Team
TRN for Mars Missions

**Terrain Relative Navigation (TRN)**
- Works by taking images during parachute descent and matching them to an onboard map
  - Uses a dedicated compute element and camera
  - Yields a position solution
- Performs terrain relative navigation while the spacecraft is priming the descent engines
- Executed by the Lander Vision System (LVS)

**Multi-Point Divert**
- Uses position solution and list of safe landing locations to select a landing target
- Augments original MSL backshell avoidance divert (requires slightly higher backshell separation altitude)
- Lives within MSL fuel and control authority constraints

Credit: JPL Mars EDL Team
More Rover Applications?

Fast traverse
Terrain mapping (while driving)
Background science (while driving)
Entry/Descent/Landing documentation (video)
  • Landing
  • Parachute release
  • Sky Crane

On-board processing for efficient use of downlink

Image Credit: JPL / MSSS MARDI Team
Real-time Mars Terrain Analysis

Figure by Garvin for MSL Science team: MARDI-based DEM derived from sidewalk video imaging mode data collection on the 22 m drive to “Book Cliffs” illustrating the power of fixed-nadir video imaging for terrain analysis of Mars in support of engineering (geotechnical) assessments.

*NOTE: DEM made from 26 overlapping MARDI video frames (nadir viewing)*
Flight Demonstrations
On-Board Image Processing

Long Range Camera on Rendezvous

Short Range Camera on Deploy

HST-SM4

GSFC SpaceCube 1.0a - Hubble SM 4 (May 2009):
• Autonomous Rendezvous and Docking Experiment
• Hosted camera AGC and two Pose algorithms

STS-125 Payload Bay

Flight Image

RNS Tracking Solution

Flight Image

RNS Tracking Solution
On-Board Image Processing

- Successfully tracked Hubble position and orientation in real-time operations
- FPGA Algorithm Acceleration was required to meet 3Hz loop requirement

→ Typical space flight processors are 25-100x too slow for this application
SMART Sounding Rocket Experiment

SpaceCube 1.5 on the SMART sounding rocket payload (SubTec-5, launched June 2011):
• Multi-function avionics
• Collaboration with ORS
SMART Video

SpaceCube 1.5 - SMART GigE Camera Clip
NASA Wallops Flight Facility - June 10, 2011
SpaceCube on the ISS

Image Credit: DoD Space Test Program
SpaceCube Overview

SpaceCube Upset Mitigation

“First” to re-program an FPGA in space!

GSFC SpaceCube 1.0b (Nov 2009):
- “Radiation Hardened by Software” Experiment (RHBS)
- Autonomous Landing Application
- Collaboration with NRL and the DoD Space Test Program (STP)

Orbit: ISS
Days in orbit: 1800+
Total SEUs detected & corrected: 200+
Total SEU-induced resets: 6
Total SEU-induced reset downtime: 30 min
Total processor availability: 99.99%
On-Orbit Upset Locations
On-Orbit Upset Locations
ISE 2.0 on ISS – August 2013
ISE 2.0 Sample Data & Images
ISEM on STP-H5 ISS Payload

The Space Test Program-H5 (STP-H5) external payload, a complement of 13 unique experiments from seven government agencies, is integrated and flown under the management and direction of the Department of Defense’s Space Test Program.

Installed on ISS February 27, 2017

ISEM Stack Includes:
- SpaceCube Mini
- FP Spectrometer
- EHD Pump
- CSP & Camera

Raven Suite Includes:
- SpaceCube 2.0
- Visible Camera
- IR Camera
- Lidar

Photo Credit: DoD STP
STP-H5 Installed on ISS - February 2017
ISEM FPS Science

- Continuous Atmospheric Methane Measurements From ISS
- Fabry-perot Spectrometer Measures Absorption By Atmospheric Gases In Sunlight Reflected Off The Earth
- Demonstrating 900:1 Downlink Data Volume Reduction
Raven Experiment Overview

Raven is a technology demonstration experiment on the Space Test Program-Houston 5 (STP-H5) payload, launched to the ISS on the SpaceX CRS-10 mission in February, 2017. During its two year mission on ISS, it will advance the state-of-the-art in NASA’s relative navigation capabilities.

- Raven contains three sensors (visible, infrared, lidar), a high-performance & reliable computing platform (SpaceCube) and advanced machine vision algorithms
- Raven tracks visiting vehicles to ISS, developing an “off-the-shelf” relative navigation capability for NASA
Raven is currently generating valuable science that is reducing the risk for future NASA missions that require rendezvous and proximity operations systems.

Dragon Tracking (VisCam)

Raven demonstrated successful on-board vehicle tracking during SpaceX CRS-10 departure.
SpaceCube Evolution and Current Research
SpaceCube Family Overview

1.0

2009  STS-125
2009  MISSE-7
2013  STP-H4
2016  STP-H5
2018  STP-H6

1.5

2012  SMART (ORS)

2.0-EM

2013  STP-H4
2016  STP-H5

2.0-FLT

2018  RRM3
2018  STP-H6 (NavCube)
2018  NEODaC
2020  Restore-L
Many NASA proposals

2.0 Mini

2016 STP-H5, UVSC-GEO, Many proposals
SpaceCube 2.0 Block Diagram

Main cPCI J1 Connector:
- PROM
- A/D
- Main Osc

Custom cPCI J2 Connector:
- RST/GPIO, 5
- GPIO/LVDS, 52
- GTX, 2x

Aeroflex UT6325 CCGA

Xilinx 0 Virtex-5
- Flash
- Flash
- SRAM
- DDR
- DDR

Xilinx 1 Virtex-5
- Main cPCI or GPIO, 60
- GTX, 2x each FPGA

Airborn 4x HS Modules
- Ethernet
- LVDS/422

Airborn Nano 85-pin
- 85-pin
- LVDS/422
- 48
- 16
- 4

Service Port

JTAG

MDM-15

SpaceCube 2.0 Highlights

Heritage

- GOAL: close the gap with commercial processors while retaining reliability
- Started in 2006 at GSFC as IR&D
- **42+ Xilinx device-years on orbit**
- 22 Xilinxes in space by 2017
- 8 systems in space by 2018
- Various R&D efforts on hardware acceleration

- Powerful hybrid data processing in a compact 3U size
- Parallel data processing:
  - FPGA + DSP + Processor(s)
- SpaceCube can move 3,000x more data than a sequential processor per clock cycle

- **Currently TRL-8**
- Leverages 10+ years of design heritage and operation experience
- **$10M+ of NRE**
- Adopted by SSPD for all missions
- **IPC 6012B Class 3/A PWB Reliability**
- Modular: 9 Mission-Unique I/O cards
- **Run-Time Reconfigurable**

Xilinx Virtex-5 FPGA

SpaceCube v2.0

SpaceCube is a Mission-Enabling Technology
SpaceCube 2.0 Processor Card

- **Power Draw:** 6-15W
- **Weight:** 0.98-lbs
- **22 Layers, Via-in-Pad**
- **IPC 6012B Class 3/A**

- 2x Xilinx Virtex-5 (QR) FX130T FPGAs
- 1x Aeroflex CCGA FPGA
  - Xilinx Configuration, Watchdog, Timers
  - Auxiliary Command/Telemetry port
- 1x 128Mb PROM, contains initial Xilinx configuration files
- 1x 16MB SRAM, rad-hard with auto EDAC/scrub feature
- 4x 512MB DDR SDRAM
- 2x 4GB NAND Flash
- 16-channel Analog/Digital circuit for system health
- Optional 10/100 Ethernet interface
- Gigabit interfaces: 4x external, 2x on backplane
- 12x Full-Duplex dedicated differential channels
- 88 GPIO/LVDS channels directly to Xilinx FPGAs
- Mechanical support for heat pipes and stiffener for Xilinx devices

2014 Mentor Graphics “Most innovative design worldwide in the Military/Aerospace sector”
Mission-Unique I/O Card Examples

- Restore-L Video/Spacecraft Interface Card
- GPS RF Front-End Interface Card
- LIDAR Digitizer, Front-End, and Laser Card
**High Level Requirements:**

- Interface with ISS and RRM3 instruments:
  - Cameras, thermal imager, motors
- Monitor/Control cryo-cooler and fuel transfer
- Stream video data
- Motor control of robotic tools
- Host Wireless Access Point
NEODaC Instrument Development

8x 3K x 3K detectors

- Near Earth Objects Detection and Characterization
  - Funded by NASA SMD/Planetary
- SerDes output drivers over 21-ft.
- SpaceCube FPGAs being used to interface with detectors, host on-board data processing applications and compression
- Successful multi-detector readout with SpaceCube completed during TVAC
- Flight system: 8 Processor Cards

SerDes Link Test Results

<table>
<thead>
<tr>
<th>Transmitter Swing (mV)</th>
<th>Transmitter % Pre-emphasis</th>
<th>Test Duration</th>
<th>Bit Error Count</th>
<th>BER (*)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500</td>
<td>0</td>
<td>6hr</td>
<td>32</td>
<td>9.2E-13</td>
</tr>
<tr>
<td>500</td>
<td>8</td>
<td>18hr</td>
<td>0</td>
<td>9.6E-15</td>
</tr>
<tr>
<td>800</td>
<td>0</td>
<td>4hr</td>
<td>4</td>
<td>1.7E-13</td>
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<td>20hr</td>
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<td>20hr</td>
<td>0</td>
<td>8.7E-15</td>
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<tr>
<td>1300</td>
<td>0</td>
<td>19hr</td>
<td>52</td>
<td>4.7E-13</td>
</tr>
</tbody>
</table>

• Note: BER calculation assumes at least 1 error
• 58-hours of error-free transmission
SpaceCube DTN Acceleration

1. FPGA IP Core to Accelerate components of the RFC 5050 Bundle Protocol (BP) Specification

2. Targets
   – SpaceCube 2.0 – Xilinx Virtex 5
   – SpaceCube 3.0 / Mustang – Microsemi RTG4

3. BP Transmission
   – Software Seeds Header Information
   – Hardware Auto Update Values and Encodes Header
   – Payload Data is DMA’d from Memory
   – Theoretical Transmission Rates
     • Virtex 5 w/ 125 Mhz Clock = 3.7 Gb/s
     • RTG4 w/ 50 MHz Clock = 1.5 Gb/s

4. BP Reception
   – Hardware decodes Header
   – Header and Payload Data are DMA’d to Memory
SpaceCube “Spin-offs” and Technology Infusion

9 Mission-Unique SpaceCube I/O Cards in various stages of integration and test

- SSCO Video Distribution Unit
- GRSSLi (Code 590)
- NavCube (Code 590)
- GEDI Digitizer design
- Complex PWB design using 1mm pitch CCGAs
  - TESS, GEDI, Mustang, OSIRIS-REx
- Proposal development
  - CycloPPS (Code 550 and Code 600)
  - DTN (Code 450)
  - DFB (Code 600)
  - Various others
- NICER/GEDI Ethernet Circuitry
Spinoff Technology Results

GPS Receiver – L1/L2C Tracking

LIDAR Instrument – Configurable Resolution

“NavCube”
- Port of “World Record Breaking” Navigator technology to SpaceCube
- Full qualification, will fly on STP-H6
- 2016 Goddard Innovation of the Year
- 6 RTAXs → ½ of 1 Virtex 5
SpaceCube Commercialization

- SpaceCube 2.0 → Genesis Engineering Solutions Inc. “GEN6000”
- NSF CHREC Space Processor → Space Micro “Cubesat Space Processor”
SpaceCube Reliability
Background Information

• Base SpaceCube unit consists of Power, Processor, and Backplane cards
• Single string SpaceCube > 99% reliability level per year (per Code 300)
• All parts can be screened to Level 1; implementing Level 2 on Restore-L
• 45+ device-years of on-orbit data shows that > 95% of all unmitigated SEUs are functionally benign
• Multiple levels of reliability and error mitigation steps can be added for mission-critical computing needs
  – Example: a 12 year MTBU embedded system is achievable for a polar orbit (~comparable to Rad750)
• Multiple mission-critical aerospace applications rely on Xilinx FPGAs
  – Examples: SLS main engine controller, commercial crew vehicle, SpaceX Dragon, Iridium constellation, Mars Lander, “other”
• The SpaceCube team has successfully tested and delivered 22 processor cards, 12 power cards, 12 backplanes (i.e. design confidence is high)
# Reliability Analysis

<table>
<thead>
<tr>
<th>Analysis</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parts Stress and De-rating</td>
<td>Complete</td>
</tr>
<tr>
<td>Signal/Power Integrity</td>
<td>Complete</td>
</tr>
<tr>
<td>Reliability Block Diagram</td>
<td>Complete (specific to Restore-L use)</td>
</tr>
<tr>
<td>Worst Case Circuit Analysis</td>
<td>Assessment Complete</td>
</tr>
<tr>
<td>FMECA</td>
<td>Complete (specific to Restore-L use)</td>
</tr>
<tr>
<td>Radiation TID Analysis</td>
<td>Complete</td>
</tr>
<tr>
<td>Radiation SEE Rate Estimation</td>
<td>Complete for Polar, ISS, Mars</td>
</tr>
<tr>
<td>Back-to-Back CGA Solder Joint Fatigue</td>
<td>Complete</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWB Coupon Tests</td>
<td>Complete – All PASS IPC 6012B 3/A</td>
</tr>
<tr>
<td>Qual TVAC/Vibe per GEVS</td>
<td>Complete - PASS</td>
</tr>
<tr>
<td>RRM3 SpaceCube TVAC/Vibe/EMI</td>
<td>Complete - PASS</td>
</tr>
<tr>
<td>“Quick-Look” EMI/EMC</td>
<td>Complete - PASS</td>
</tr>
<tr>
<td>4x CGA Life Test Articles (-55/+100C)</td>
<td>Ongoing - &gt; 5x MoS factor achieved</td>
</tr>
</tbody>
</table>
# Reliability Spectrum (It’s your choice)

<table>
<thead>
<tr>
<th>Reliability</th>
<th>Radiation Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Box redundancy</td>
<td>Full TMR/NMR</td>
</tr>
<tr>
<td>Card redundancy</td>
<td>Selective mitigation</td>
</tr>
<tr>
<td>Internal redundancy</td>
<td>DDR ECC</td>
</tr>
<tr>
<td>Higher Part levels (3→2→1)</td>
<td>Fault-Tolerant processor</td>
</tr>
<tr>
<td>Single string</td>
<td>Xilinx device type</td>
</tr>
</tbody>
</table>

**The systems trades: Computing Performance vs. Radiation Performance**

(adding levels of radiation tolerance requires some level of resources)

**Mission Examples (low end to high end, in order of increasing cost):**

- Tech Demo (Do no harm): ISS, Single string, “EDU” parts, Config scrubbing, Flash ECC, Defense-grade Xilinx using PowerPCs
- Class C: Level 2 parts, some redundancy, DDR ECC, FT processor for critical tasks, selective mitigation
- Class A/B critical function: Level 1 parts, Box redundancy, FT processor, memory EDAC, possibly full TMR
NASA Risk Assessment

Establishing Acceptable SEE Error Rates Using a Risk-based Engineering Analysis Approach

### Assessment Process

- **Radiation Environment**
- Establish Device WCA
- Establish System WCA
- Establish Application WCA
- ID Functional Independence
- Selective FPGA Mitigation

### Likelihood of Safety Event

<table>
<thead>
<tr>
<th>Likelihood</th>
<th>Safety Event Likelihood</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 Very High</td>
<td>$P_{SE} &gt; 10^{-1}$</td>
</tr>
<tr>
<td>4 High</td>
<td>$10^{-2} &lt; P_{SE} \leq 10^{-1}$</td>
</tr>
<tr>
<td>3 Moderate</td>
<td>$10^{-3} &lt; P_{SE} \leq 10^{-2}$</td>
</tr>
<tr>
<td>2 Low</td>
<td>$10^{-5} &lt; P_{SE} \leq 10^{-3}$</td>
</tr>
<tr>
<td>1 Very Low</td>
<td>$10^{-6} &lt; P_{SE} \leq 10^{-5}$</td>
</tr>
</tbody>
</table>

### Technical Requirements

<table>
<thead>
<tr>
<th>Likelihood</th>
<th>Technical Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 Very High</td>
<td>$P_{T} &gt; 50%$</td>
</tr>
<tr>
<td>4 High</td>
<td>$25% &lt; P_{T} \leq 50%$</td>
</tr>
<tr>
<td>3 Moderate</td>
<td>$15% &lt; P_{T} \leq 25%$</td>
</tr>
<tr>
<td>2 Low</td>
<td>$2% &lt; P_{T} \leq 15%$</td>
</tr>
<tr>
<td>1 Very Low</td>
<td>$0.1% &lt; P_{T} \leq 2%$</td>
</tr>
</tbody>
</table>

### Estimated Restore WCA Upset Rates

<table>
<thead>
<tr>
<th>Mode</th>
<th>Time (s)</th>
<th>Device WCA Utilization</th>
<th>PCC WCA Utilization</th>
<th>RPO PCC</th>
<th>RSW PCC</th>
<th>RPO + RSW PCC</th>
</tr>
</thead>
<tbody>
<tr>
<td>one orbit (96 min)</td>
<td>5760</td>
<td>0.484%</td>
<td>1.934%</td>
<td>1.074%</td>
<td>0.222%</td>
<td>1.296%</td>
</tr>
<tr>
<td>Rendezvous (30 min)</td>
<td>1800</td>
<td>0.151%</td>
<td>0.604%</td>
<td>0.336%</td>
<td>0.069%</td>
<td>0.405%</td>
</tr>
<tr>
<td>Capture (77 sec)</td>
<td>77</td>
<td>0.006%</td>
<td>0.026%</td>
<td>0.014%</td>
<td>0.003%</td>
<td>0.017%</td>
</tr>
</tbody>
</table>

- Note: assumes BRAM Mitigation
- Note: Actual utilization for RPO and RSW PCCs as of 4/18/2016
- Note: assumes RPO & RSW PCCs must be error-free for full operation

<0.1% = not a credible risk
Flight Tested Mitigation Techniques

- Self-scrubber internally TMR’d on every SpaceCube 1.0 flight mission/demo (STS-125, MISSE, STP-H4, STP-H5, STP-H6) ... Total of ~37 device-years in orbit
- MISSE-7 Reed-Muller EDAC memory controller and dual processor configuration where each processor had a time window to report its answer to voting processor ... MISSE-7 SpaceCube operated for 7.3 years
- ISE 2.0 Xilinx Virtex-5 FPGA 1 performed self-scrubbing using files stored in NAND Flash memory and configured/scrubbed the configuration memory of Xilinx FPGA 2 and Xilinx FPGA 3. Xilinx FPGA1 counted the number of detected and corrected configuration memory upsets for all 3 FPGAs using the internal CRC Readback feature of the Xilinx configuration controller. FPGA1’s configuration file was stored in a rad-hard PROM which configured the FPGA on power up.
- ISEM rad-hard watchdog FPGA performed configuration/scrubbing of the Xilinx Virtex-5 FPGA. The rad-hard FPGA counted the number of detected and corrected configuration memory upsets for the Xilinx FPGA using the internal CRC Readback feature of the Xilinx configuration controller. Robust page-level and file-level redundancy and error detection were used to ensure the configuration files stored in the NAND Flash memory could be reconstructed despite radiation-induced upsets.
- RRM3 boot-up configuration files stored in radiation hardened PROM. Initial boot-up configuration is performed by a rad-hard FPGA. The rad-hard FPGA also monitors watchdog signals from the Xilinx FPGAs and will reconfigure them with the boot-up configuration files if the watchdogs aren’t serviced. Multiple redundant flight configuration files are stored in the NAND Flash. Xilinx FPGA1 detects, counts, and corrects upsets on Xilinx FPGA2. Xilinx FPGA2 receives the FPGA1 configuration file from FPGA1 and stores it in local memory. FPGA2 detects, counts, and corrects upsets on FPGA1 so long as the configuration file in local memory remains valid.

*Note: In general, TMR and EDAC is platform agnostic. The mitigation techniques themselves have heritage, and that’s what is important.
Mitigation Analysis Example

- In a worst-case GEO environment a Xilinx Virtex-5 PLL has a recoverable error Mean Time Between Upset (MTBU) of 82 years. The Xilinx PLL does not have an error condition that requires a reconfiguration or power cycle.
- The RTG4 PLL rad report for the same orbit (GEO solar-min behind 100mil Al) states a Recoverable error MTBU of 33 years and Error requiring a reset MTBU of 6,850 years.
- “Both PLLs are rock solid. As a note, we currently have 15 PLLs in use on the Restore-L payload spread among 5 subsystems. Our Polar environment is about twice as bad as GEO given the proton densities.”

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Recoverable Error MTBU</th>
<th>Error Requiring Reset MTBU</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTG4</td>
<td>33 years</td>
<td>6850 years</td>
</tr>
<tr>
<td>Xilinx V5</td>
<td>82 years</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Source Data:
https://www.microsemi.com/document-portal/doc_download/137654-rtg4 pll and internal oscillator see report

- The SpaceCube processor card can be populated with the space-grade Xilinx devices (QV/SIRF), and critical logic can be TMR’d if need be. A fault tolerant MicroBlaze processor coupled with the rad-hard SRAM yields a core processing system with a MTBU of 13 years, which is comparable to the RAD750.
- A hybrid approach where one Xilinx is rad-hard and the other is defense-grade gives the application access to dual PowePCs 440s capable of 1500 DMIPs each, in addition to the rad-hard FPGA resources.
Software Techniques: Application of Time & Space Partitioning for Additional SpaceCube Fault Tolerance

• Combining a mix of rad-hard FPGAs with rad-tolerant FPGAs along with Time and Space partitioning provides additional fault tolerance with minimal impact on system performance
  – Time-Triggered Architecture (TTA)
    • Processing tasks are executed according to a pre-determined schedule
  – Time and Space Partitioning (TSP)
    • Processing tasks are executed according to a pre-determined schedule and isolated in address space such that a task cannot modify another tasks data or code

• Flexible SpaceCube architecture allows a two-sided card with a Space-grade Virtex-5QV FPGA on one side mated with an industrial grade Virtex-5 FPGA on the other
  – Virtex-5QV running MicroBlaze™ processor(s)
  – Virtex-5 with dual 440 Power PC processors

• Software application execution is synchronized to the critical data Input/Output schedule across all processors on a time triggered subnetwork
  – High performance processing is run redundantly and in parallel on 2 or more PPC processors
  – I/O voting and/or agreement algorithms are handled by Virtex-5QV MicroBlaze™ processor(s)
  – On miscompare, Rad-Hard MicroBlaze™ performs fault handling
    • MicroBlaze™ can retain state or checkpoint data for rapid recovery of system
    • MicroBlaze™ can perform safehold algorithms as needed
Software Demonstrations: Examples of Time & Space Partitioning in Fault Tolerant Systems

- Upcoming UVSC/NRL GEO flight experiment on SpaceCube
  - Redundant/parallel data processing synchronized to schedule with outputs voted on by independent processors
  - Hard-Real time performance, fault detection and handling
- Successful NASA/JSC demonstration of quad redundant architecture using NASA Core Flight System (cFS) software architecture (2 fault and byzantine tolerant)
  - Voted signed commands and state exchange over Time-Triggered Ethernet (TTE) subnetwork
  - All application processing synchronized to TTE schedule
  - Hard-Real time performance, fault detection and handling
On-going and Future Work
Restore-L Avionics

High Level Requirements:

- Interface with Spacecraft and Payload Busses
- Interface with vision sensors
- Host Relative Proximity Operations application
- Host Robotic Manipulation Control application

Restore-L will fly 21 Xilinx Virtex-5 FPGAs
Restore-L Capture and Refuel Video
Ultraviolet Spectro-Coronagraph Pathfinder

The NRL UVSC Pathfinder combines an ultra-violet spectrograph with a novel, high-throughput coronagraph to search for the presence of suprathermal seed particles near the sun. These particles are believed to be necessary for the production of large solar energetic particle (SEP) events.

- Scheduled to fly in 2019 on STPSat6
- SpaceCube Mini serves as the UVSC instrument processor
- Hybrid high-performance fault-tolerant software architecture
- First flight of SpaceCube technology in a GEO orbit

The largest SEP events are thought to be produced when shocks created by fast-moving coronal mass ejections (CMEs) interact with a pre-existing population of seed particles. UVSC will detect the signature of these seed particles by measuring enhancements of the wings of the hydrogen Lyman alpha spectral line. The coronagraph section blocks the solar disk light to allow the corona to be imaged at 1.8 and 3 solar radii, which is the region where CME shocks are first formed.

SEP events disrupt Navy/DoD space operations with little or no warning by damaging critical spacecraft sub-systems. UVSC will demonstrate a new capability that will extend the warning time for SEP events and thereby allow time for mitigating the effects of these hazards.
SpaceCube 2.0 Micro

Top Side

Bottom Side, looking through top
SpaceCubeX End-to-End Framework

End to end tools which enable rapid, accurate exploration of on-board computing architectures
SpaceCubeX: Performance Comparison

Performance Analysis for SpaceCubeX Architectures

Hybrid Multi-Core/FPGA Architectures provides orders of magnitude higher performance

*Simulation performance verified to be accurate within 1%-6% via emulation testing
SpaceCube 3.0 Architecture

I/O
- Multi-Gigabit Science Data
- Ethernet
- RS-422/LVDS

Memory
- High-Speed Volatile Memory
- High-Speed Volatile Memory
- Non-Volatile Memory
- Non-Volatile Memory

System Monitor
- Radiation Hardened FPGA

Processing Elements
- High-Performance FPGA-1
  - FPGA DSP Logic, Embedded Soft-core CPUs
- High-Performance Multi-Core CPU
- Expansion Plug-in Module

High-Performance FPGA-2
- FPGA DSP Logic, Embedded Soft-core CPUs

Multi-Many Core CPU / High Performance Space Computer (HPSC)

High-speed A/D or other module
Conclusions

SpaceCube is a MISSION ENABLING technology

- Delivers 10x to 100x on-board computing power
- Cross-cutting (Earth/Space/Planetary/Exploration)
- Being reconfigurable equals BIG SAVINGS
- SpaceCube can be used in all mission applications
  ... up to and including Class A
- Past research / missions have proven viability
- Ready for infusion into operational missions
The SpaceCube Team
Thank you! Questions?

tom.flatley@nasa.gov
spacecube.nasa.gov

Special thanks to our sponsors: NASA/GSFC IR&D, NASA Satellite Servicing Programs Division (SSPD), NASA Earth Science Technology Office (ESTO), DoD Space Test Program (STP), DoD Operationally Responsive Space (ORS)
## Acronyms

<table>
<thead>
<tr>
<th>A/D</th>
<th>Analog to Digital converter</th>
<th>IR</th>
<th>Infra Red</th>
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<tbody>
<tr>
<td>AGC</td>
<td>Automatic Gain Control</td>
<td>ISE 2.0</td>
<td>ISS SpaceCube Experiment 2.0</td>
</tr>
<tr>
<td>ATCORR</td>
<td>Atmospheric Correction</td>
<td>ISEM</td>
<td>ISS SpaceCube Experiment - Mini</td>
</tr>
<tr>
<td>CFE/CFS</td>
<td>Core Flight Executive / Core Flight Software</td>
<td>ISS</td>
<td>International Space Station</td>
</tr>
<tr>
<td>CHREC</td>
<td>NSF Center for High-performance Reconfigurable Computing</td>
<td>LEO</td>
<td>Low Earth Orbit</td>
</tr>
<tr>
<td>CIB</td>
<td>Communications Interface Box</td>
<td>LIDAR</td>
<td>Light Detection and Ranging</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
<td>MARDI</td>
<td>Mars Descent Imager</td>
</tr>
<tr>
<td>CRS</td>
<td>Cargo Re-Supply</td>
<td>MIPS</td>
<td>Million Instructions Per Second</td>
</tr>
<tr>
<td>CSP</td>
<td>CHREC Space Processor</td>
<td>MISSE</td>
<td>Materials on the International Space Station</td>
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<td>DEM</td>
<td>Digital Elevation Map</td>
<td>MSL</td>
<td>Mars Science Laboratory</td>
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<tr>
<td>DoD</td>
<td>Department of Defense</td>
<td>NASA</td>
<td>National Aeronautics and Space Administration</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
<td>NEODAC</td>
<td>Near Earth Object Detection And Characterization</td>
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<tr>
<td>EDL</td>
<td>Entry, Descent, Landing</td>
<td>NSF</td>
<td>National Science Foundation</td>
</tr>
<tr>
<td>EHD</td>
<td>Electro-Hydro Dynamic</td>
<td>ORS</td>
<td>Operationally Responsive Space</td>
</tr>
<tr>
<td>ELC</td>
<td>ISS Express Logistics Carrier</td>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>EM</td>
<td>Engineering Model</td>
<td>RNS</td>
<td>Relative Navigation System</td>
</tr>
<tr>
<td>EMD</td>
<td>Empirical Mode Decomposition</td>
<td>RRM</td>
<td>Robotic Refueling Mission</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
<td>SAR</td>
<td>Synthetic Aperature Radar</td>
</tr>
<tr>
<td>FPS</td>
<td>Fabry-Perot Spectrometer</td>
<td>SEP</td>
<td>Solar Energetic Particle</td>
</tr>
<tr>
<td>FPU</td>
<td>Floating Point Unit</td>
<td>SM4</td>
<td>HST Servicing Mission 4</td>
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<td>GEO</td>
<td>Geosynchronous Orbit</td>
<td>SMART</td>
<td>Small Rocket/Spacecraft Technology</td>
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<td>GigE</td>
<td>Gigabit Ethernet</td>
<td>SSPD</td>
<td>NASA GSFC Satellite Servicing Projects Division</td>
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<td>GNFIR</td>
<td>Goddard Natural Feature Image Recognition</td>
<td>STMD</td>
<td>NASA Space Technology Mission Directorate</td>
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<td>GOES</td>
<td>Geostationary Operational Environmental Satellites</td>
<td>STP</td>
<td>DoD Space Test Program</td>
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<td>GSFC</td>
<td>NASA Goddard Space Flight Center</td>
<td>STS</td>
<td>Space Transportation System (Shuttle)</td>
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<tr>
<td>HHT</td>
<td>Hilbert-Huang Transform</td>
<td>TRN</td>
<td>Terrain Relative Navigation</td>
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<tr>
<td>HPFEC</td>
<td>High-Performance Fault-Tolerant Embedded Computing benchmarks</td>
<td>UVSC</td>
<td>Ultra Violet Spectral Chronograph</td>
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<tr>
<td>HPSC</td>
<td>High Performance Space Computer</td>
<td>WFF</td>
<td>NASA Wallops Flight Facility</td>
</tr>
<tr>
<td>HST</td>
<td>Hubble Space Telescope</td>
<td></td>
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