SpaceCube v3.0 Mini
NASA Next-Generation Data-Processing System
for Advanced CubeSat Applications

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## Acronyms

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<th>Acronym</th>
<th>Definition</th>
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<tr>
<td>BL-TMR</td>
<td>BYU-LANL TMR</td>
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<tr>
<td>cFE</td>
<td>Core Flight Executive</td>
</tr>
<tr>
<td>cFS</td>
<td>Core Flight System</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>CSP</td>
<td>CHREC/CubeSat Space Processor</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>FF</td>
<td>Flip-Flop</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>FSM</td>
<td>Finite State Machine</td>
</tr>
<tr>
<td>ISA</td>
<td>Instruction Set Architecture</td>
</tr>
<tr>
<td>LEO</td>
<td>Low-Earth Orbit</td>
</tr>
<tr>
<td>MGT</td>
<td>Multi-Gigabit Transceiver</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>RE</td>
<td>Recurring Engineering</td>
</tr>
<tr>
<td>SBC</td>
<td>Single-Board Computer</td>
</tr>
<tr>
<td>SEL</td>
<td>Single-Event Latchup</td>
</tr>
<tr>
<td>SEM</td>
<td>Soft Error Mitigation</td>
</tr>
<tr>
<td>TID</td>
<td>Total Ionizing Dose</td>
</tr>
<tr>
<td>TMR</td>
<td>Triple Modular Redundancy</td>
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Outline

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4. SpaceCube v3.0 Mini
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## Goals, Motivations, Challenges

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<th>Goals</th>
<th>Motivations</th>
<th>Challenges</th>
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<tr>
<td>Develop reliable, high-speed hybrid processor using <strong>SpaceCube design approach</strong> to enable next-generation instrument and CubeSat capability</td>
<td>Many commercial CubeSat processor offerings primarily target benign LEO orbits and <strong>do not strongly address</strong> radiation concerns and parts qualification. Need exceptional capability to support complex applications such as artificial intelligence.</td>
<td>Managing PCB area restrictions for rad-hard components, balancing cost, educating mission designers for key reliability differences.</td>
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SpaceCube Introduction

What is SpaceCube?
A family of NASA developed space processors that established a **hybrid-processing approach** combining radiation-hardened and commercial components while emphasizing a novel architecture **harmonizing** the best capabilities of CPUs, DSPs, and FPGAs.

High performance reconfigurable science / mission data processor based on Xilinx FPGAs
- Hybrid processing …
  - CPU, DSP, and FPGA logic
- Integrated “radiation upset mitigation” techniques
- SpaceCube “core software” infrastructure (cFE/cFS and “SpaceCube Linux” with Xenomai)
- Small “critical function” manager/watchdog
- Standard high-speed (multi-Gbps) interfaces
SpaceCube Heritage

Closing the gap with commercial processors while retaining reliability

- 57+ Xilinx device-years on orbit
- 26 Xilinx FPGAs in space to date (2019)
- 11 systems in space to date (2019)

SpaceCube is Mission Enabling...

SpaceCube v1.0
- STS-125, MISSE-7, STP-H4, STP-H5, STP-H6

SpaceCube v1.5
- SMART (ORS)

SpaceCube v2.0-EM
- STP-H4, STP-H5

SpaceCube v2.0-FLT
- RRM3, STP-H6 (NavCube)

SpaceCube v2.0 Mini
- STP-H5, UVSC-GEO
SpaceCube Approach

01. The traditional path of developing radiation-hardened flight processor **will not work** ... they are always one or two generations behind.

02. Use latest radiation-tolerant* processing elements to achieve massive **improvement** in “MIPS/watt” (for same size/weight/power).

03. Accept that radiation induced upsets may happen occasionally and just deal with them appropriately ... any level of reliability can be achieved via **smart system design**!

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*Radiation tolerant – susceptible to radiation induced upsets (bit flips) but not radiation-induced destructive failures (latch-up)*
Mini Design Philosophy

**SpaceCube v3.0 Processor Card**

- **Same Approach, Smaller Size**
  - SpaceCube design approach applied to smaller form-factor

- **Key Design Reused**
  - Much of UltraScale design and interface remain same between cards including DDR Pinout

**SpaceCube v3.0 Mini**

- **Supervision Requested**
  - Radiation-hardened monitor architecture and code reusable

- **Trade in, Trade Out**
  - EEE parts trades, analysis, and circuits extensively leveraged from main card design
Mini Form Factor Lessons Learned

**Manufacturability**
Difficult to manufacture due to rigid-flex and laser-drilled microvias. Tied to single vendor design.

**Monitor Design**
Aeroflex rad-hard monitor was effective, however, limited by FPGA resources preventing more robust design.

**CubeSat Connector**
Samtec SEARAY connector provided flexibility and performance, same connector used with SpaceVNX (VITA 74.4)

**Backplane Advantage**
Backplane allows swapping of individual card as advances/improvements are made and can easily incorporate new components.

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*SpaceCube Mini v2.0 Lessons Learned*

*CSPv1 Lessons Learned*
SmallSat/CubeSat Processor Challenge

Massively Expanding Commercial Market for SBCs
- Tons of commercial vendors in CubeSat Market (e.g. Pumpkin, Tyvak, GomSpace, ISIS, Clyde Space, etc…)

Mission Developers Seeking Commercial Hardware
- Under pressure from cost-cap missions, and reducing costs in general
- Reduced RE for constellation mission concepts
- Attractive all-commercial solutions provided integrating several CubeSat “Kit” types of cards

Not Designed With Harsh Orbit Considerations Beyond LEO
- Many vendors have performed limited radiation testing and largely support missions in more benign LEO orbits
- Mission is radiation test approach
- Little-to-no additional radiation testing or parts qualification
- No recommendations for fault-tolerant configurations of offered SBCs

## Xilinx Space Devices Compared

<table>
<thead>
<tr>
<th>Resource</th>
<th>SpaceCube v1.0</th>
<th>SpaceCube v2.0</th>
<th>SpaceCube v3.0</th>
<th>KU060 vs. V5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells</td>
<td>56,880</td>
<td>142,128</td>
<td>131,072</td>
<td>726,000</td>
</tr>
<tr>
<td>CLB FF</td>
<td>50,560</td>
<td>126,336</td>
<td>81,920</td>
<td>663,360</td>
</tr>
<tr>
<td>Max Distributed RAM (Kb)</td>
<td>395</td>
<td>987</td>
<td>1,580</td>
<td>9,180</td>
</tr>
<tr>
<td>Total Block RAM (Kb)</td>
<td>4,176</td>
<td>9,936</td>
<td>10,728</td>
<td>38 Mb</td>
</tr>
<tr>
<td>BRAM/FIFO ECC (36 Kb)</td>
<td>--------------</td>
<td>---------------</td>
<td>---------------</td>
<td>--------------</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>128</td>
<td>192</td>
<td>320</td>
<td>2,760</td>
</tr>
<tr>
<td>MGT</td>
<td>18 @ 4.25 Gbps</td>
<td>32 @ 12.5 Gbps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TID (krad)</td>
<td>300</td>
<td>300</td>
<td>1,000</td>
<td>120</td>
</tr>
<tr>
<td>SEL</td>
<td>&gt;125</td>
<td>&gt;125</td>
<td>&gt;125</td>
<td>∼80</td>
</tr>
<tr>
<td>Flow</td>
<td>V-Flow (QML-V)</td>
<td>B-Flow (QML-Q)</td>
<td>B-Flow (QML-Q)</td>
<td>N/A</td>
</tr>
<tr>
<td>Package</td>
<td>35 x 35 mm</td>
<td>40 x 40 mm</td>
<td>45 x 45 mm</td>
<td>40 x 40 mm</td>
</tr>
</tbody>
</table>

"Xilinx’s Adaptive FPGAs for Space Applications” White Paper
Xilinx Kintex UltraScale XQRKU060

• First 20 nm FPGA for Space
  – Designed for SEU mitigation (>40 patents)
  – Deploys same commercial silicon mask set
  – Uses Vivado UltraFast Development

• Ruggedized 1509 CCGA
  – 40 mm x 40mm package
  – Footprint compatible A1517

• Product Space Test Flows
  – B-Flow (QML-Q Equiv.) and Y-Flow (QML-Y Compliant)

• Commercial Radiation Testing Results
  – Improved Xsect compared to 7 series
  – No observed classical SEL signatures


Fault-Tolerant Soft-Core Processing

**Xilinx TMR MicroBlaze**
- Built-in Xilinx TMR solution for newer FPGAs
- Includes TMR SEM IP Core
- Vivado IP integrator for easy project creation

**BL-TMR MicroBlaze**
- BYU-LANL TMR Tool (BL-TMR) provides automated TMR application
- Fault Injection on MicroBlaze performed for SpaceCube v2.0

**BL-TMR RISC-V**
- RISC-V is a promising new ISA processor gaining popularity for Intel and Xilinx FPGAs
- Neutron radiation test of Taiga RISC-V
- 27% decrease in operational frequency, for 33x improvement in cross section

### Resource Utilization of TMR Designs on KU040

<table>
<thead>
<tr>
<th>Resource</th>
<th>MicroBlaze Stand Alone</th>
<th>Xilinx TMR MicroBlaze</th>
<th>BL-TMR MicroBlaze</th>
<th>BL-TMR RISC-V</th>
</tr>
</thead>
<tbody>
<tr>
<td>LUTs</td>
<td>3.29%</td>
<td>9.81%</td>
<td>15.58%</td>
<td>0.80%</td>
</tr>
<tr>
<td>CLB FF</td>
<td>1.63%</td>
<td>4.77%</td>
<td>4.89%</td>
<td>0.20%</td>
</tr>
<tr>
<td>BRAM/FIFO ECC (36 Kb)</td>
<td>12.50%</td>
<td>37.50%</td>
<td>37.50%</td>
<td>1.00%</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>0.31%</td>
<td>0.94%</td>
<td>0.94%</td>
<td>0.20%</td>
</tr>
<tr>
<td>FMax</td>
<td>-----</td>
<td>0.95x</td>
<td>0.88x</td>
<td>0.73x</td>
</tr>
</tbody>
</table>

BL-TMR v6.3, MicroBlaze v11, 32-bit 5-stage, FPU, 32 Kb I/D, Vivado 2019.1,

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2. [http://reliability.ee.byu.edu/edif/](http://reliability.ee.byu.edu/edif/)

SCv3.0 Mini Booting Configuration

Selectable Configuration
- Kintex configured via SelectMAP from backplane or on-board RTProASIC3 supervisor
- Dozens of configuration files stored with redundant copies across multiple internal dies

Robust RTProASIC Monitor
- Verifies configuration files are valid via page-level CRC checks
- Can reconstruct valid configuration file from several corrupted ones
- Internal FSM ensures Kintex programming and boot sequence is completed correctly
- Automatic program retry

Flexible Configuration
- Can be reconfigured via command from spacecraft to ProASIC
- Can change configurations in-flight to support dynamic mission requirements
SCv3.0 Mini Fault-Tolerant Architecture

Stand-Alone Operation (RT-ProASIC)
- Scrubs Kintex configuration during operation via either:
  - Blind scrubbing (consistent time interval)
  - Smart scrubbing (readback scrubbing to check configuration and correct errors as they are detected)
- Scrubs configuration files in NAND flash memory

Companion-Card Operation (GSFC CubeSat Bus)
- Combines reliability of RTG4 with high performance of SCv3Mini to form flexible, reusable SmallSat/CubeSat bus
- RTG4 configures and monitors Mini over the backplane

![Diagram of SCv3.0 Mini Fault-Tolerant Architecture](image-url)
SCv3.0 Mini High-Level Specifications

Overview

- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0
- High-performance processor of Goddard’s modular CubeSat spacecraft bus Dellingr-X

High-Level Specifications

**1x Xilinx Kintex UltraScale**
- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 30x 3.3V GPIO
  - 2 RS-422/LVDS
  - SelectMAP Interface
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG
Conclusions

SpaceCube is a MISSION ENABLING technology

• Delivers exceptional on-board computing power
• Cross-cutting (Earth/Space/Planetary/Exploration)
• Being reconfigurable equals BIG SAVINGS
• SpaceCube can be used in all mission applications
  ... up to and including Class A
• Past research / missions have proven viability
• Ready for infusion into operational missions
• Next-Generation CubeSat design for artificial intelligence and machine learning applications
Thank you! Questions?

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