Experimental Study on Mitigation of Lifetime-Limiting Dielectric Cracking in Extreme Temperature 4H-SiC JFET Integrated Circuits

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Abstract. While NASA Glenn Research Center’s “Generation 10” 4H-SiC Junction Field Effect Transistor (JFET) integrated circuits (ICs) have uniquely demonstrated 500 °C electrical operation for durations of over a year, this experimental work has also revealed that physical cracking of chip dielectric passivation layers ultimately limits extreme-environment operating lifetime [1-3]. The prevention of such dielectric passivation cracks should therefore improve IC high temperature durability and yield, leading to more beneficial technology adoption into aerospace, automotive, and energy systems. This report describes Generation 10.2, 11.1, and 11.2 die tested under unbiased and unpackaged accelerated age testing at 500 °C, 600 °C, 720 °C, and 800 °C in air-atmosphere ovens for 100- and 200-hour duration. Additional samples were separately subjected to 10 thermal cycles between the same high temperatures (with 10-hour high-temperature soak each cycle) and 50 °C. It is shown that having two stoichiometric Si3N4 layers in the interconnect dielectric stack substantially decreases the amount of dielectric cracking observed following these oven tests.

Introduction

NASA Glenn Research Center has focused over the last few decades to develop IC electronics for aeronautics and space applications that can operate durably for prolonged time at 500 °C. This temperature regime is dictated by the fact that Venus surface conditions are 462 °C and jet engine’s wall temperature at the outlet of the compressor typically do not go above 500 °C. The current research effort has relied on 4H-SiC n-channel JFETs and matching 4H-SiC n-type resistors (JFET-R) which can endure the extreme environment [1-3] while simultaneously enabling constant-bias operation across the temperature (T) range from -190 °C (near cryogenic liquid nitrogen T) to +960 °C [4]. Improvements in circuit design focused on being insensitive to variations in Vt and lower power consumptions while not pushing classic chip metrics such as switching speed. Increasingly capable consecutive generations of SiC JFET-R ICs and packaging prototyped by NASA Glenn have recently culminated in demonstrations of nearly 200 transistor Generation 10 IC chips (from two wafers denoted 10.1 and 10.2) operating for over a year at 500 °C in Earth air ambient [2] and for 60 days in a Venus surface condition test chamber [5].

There are four reasons why testing above 500 °C is important for achieving durable 500 °C electronics infusion. First, elevated (higher than intended application) operating temperatures are an accepted method of accomplishing accelerated age testing as long as there’s no phase transition in any of the materials at the elevated temperatures of the testing. Second, it is important to understand chip thermal limits for packaging purposes. For example, the current NASA Glenn high temperature packaging technology relies upon a gold sintering process that is done at 600 °C [6]. Additionally, one could apply alternative packaging techniques, perhaps including additive manufacturing, so long as thermal budgets fall within the known thermal limits of the die. Third, additional applications, such as in turbine engines and hypersonic flight, could possibly benefit considerably from ICs surviving...
short duration excursions above 500 °C. Lastly, it is humanity’s inquisitive nature to push a technology to its failure which improves basic understanding of the failure modes.

This paper focuses on preventing dielectric cracking at temperatures from 500 °C to 800 °C via annealing studies conducted on unpackaged chips diced from Generation 10 and Generation 11 prototype wafers (denoted 10.2, 11.1, and 11.2). This paper found three ways of preventing dielectric cracking at temperatures from 500 °C to 800 °C: (1) the addition of more than one stoichiometric Si$_3$N$_4$ layer to the IC dielectric interconnect stack, (2) the patterned etch removal of all dielectrics in the SiC dicing-saw path, and (3) the introduction of a metal “fence” patterns that can affect lateral propagation dielectric cracks.

**Device Structure: Wafers 10.2, 11.1, and 11.2**

Fig. 1 Shows a Focused Ion Beam (FIB) Field Emission Scanning Electron Microscope (FE-SEM) cross-sectional image from wafer 10.2 that illustrates the fundamental SiC interconnect approach implemented on NASA prototype IC Generations 8 through 11. For clarity on nomenclature; the generation is the integer value, whereas after the decimal represents a specific wafer identification associated with unique interconnect process flow. It is important to note (counterintuitively) that interconnect processing of 11.1 took place after completion and cross-sectional analysis of wafer 11.2. A stoichiometric Si$_3$N$_4$ layer is sandwiched between the upper two 1.0 µm oxide layers (i.e., the two oxide layers above Metal 2) for all three wafers studied. The Metal 1 and Metal 2 layers for 10.2 and 11.2 were close-proximity sputter-deposited by pulsed DC at 3.5mTorr Ar as described in [3]. The resulting TaSi$_2$ was sufficiently dense over topology for 10.2 to allow two levels of durable interconnect that enabled considerably improved circuit density and chip layout over sign level interconnects. Except for ion implantation and Si$_3$N$_4$ layer deposition, all processing was carried out at NASA Glenn starting from commercially purchased 76
mm diameter SiC epi-wafers [7]. In as-fabricated die, only the TaSi2/Pt/Ir/Pt (400/200/200/200nm) + 1 µm Au metal stack deposited directly on SiC as topside chip bonding pads [8,9] and chip backside blanket metallization are exposed to atmosphere. Metal 1 and Metal 2 interconnects are buried in their entirety beneath the upper SiO2/Si3N4/SiO2.

Fig. 2 shows a FIB FE-SEM cross-sectional image of Wafer 11.2 that illustrates a Metal 2 interconnect trace residing above a crossing underlying Metal 1 trace formed above a flat SiC field region (i.e., a region of the chip without underlying SiC mesa etch topography). It is vitally important to note that 11.2 was the only wafer in this report to include a lower Si3N4 layer (sandwiched by 0.5 µm SiO2 layers) residing between Metal 1 and Metal 2 (as seen in the Fig. 2). Illustrated with a red arrow in Fig. 2(a) is a crack with metal void feature that resulted in undesired open-circuiting of many Metal 2 interconnect traces, which led to poor overall electrical circuit yield on 11.2. Fig. 2(b) shows a higher magnification view of this crack revealing that the Si3N4 is present (i.e., partly deposited) in the upper SiO2. This indicates that the crack occurred during loading (warm-up) prior to the start of the stoichiometric Si3N4 layer deposition.

Based upon the above results from wafer 11.2, it was decided to alter the TaSi2 metal deposition process to attempt to achieve improved metal film properties towards eliminating Metal 2 crack formation at topologic features. An un-optimized process of High-Power Impulse Magnetron Sputtering (HiPIMS) [10] was implemented for Metal 1 and Metal 2 for 11.1. Additionally, amid concern that the stress in the dielectrics might have contributed to the observed Metal 2 crack formation in 11.2, Wafer 11.1 was subsequently processed with only one Si3N4 layer (above Metal 2). The layer cross-sectional differences of this study are represented by simplified icon images at the bottom-left of Table 1. Except for the difference in metal sputter deposition technique, the entire interconnect/dielectric stack of 11.1 is the same (layer thicknesses and materials) as 10.2.

As seen in Fig. 4, the mask/circuit patterns and chip sizes were significantly different between the 10 and 11 prototype generations. Wafer 10.2 had two different 3 mm x 3 mm chip layout designs tested in this experiment, illustrated in the photos of Fig. 4(a) “Analog to Digital” chip (with three vertical Metal 1 power bus traces along left side) and Fig. 4(b) “÷2/÷4 Clock” chip (with more-centered power bus traces) [11]. For 11.1 and 11.2 respectively shown in Fig. 4(c) and 4(d), the same “Shift Register” 4.65 mm x 4.65 mm chip design was studied (with three larger Metal 1 power bus traces near the middle).

**Table 1 Thermal Chip Annealing Results Summary**

| Version 10.2 | C1 | 500 | 600 | 720 | 800 | °C | Version 11.1 | C7 | 500 | 600 | 720 | 800 |
|--------------|----|-----|-----|-----|-----|----|--------------|----|-----|-----|-----|-----|----|
| Analog to Digital | 100 hours | 1 | 1 | 3 | 3 | 0 | 100 hours | 3 | 3 | 3 | 3 | 0 |
| 10-10hr cycle | 1 | 2 | 3 | 3 | 0 | 2 | 3 | 3 | 3 | 0 | 2 | 3 |

| Version 10.2 | C3 | 500 | 600 | 720 | 800 | °C | Version 11.1 | C7 | 500 | 600 | 720 | 800 |
|--------------|----|-----|-----|-----|-----|----|--------------|----|-----|-----|-----|-----|----|
| Clock ÷2 ÷4 | 100 hours | 1 | 0 | 3 | 0 | 0 | 100 hours | 0 | 0 | 0 | 1 | 0 |
| 10-10hr cycle | 1 | 2 | 3 | 0 | 0 | 2 | 0 | 0 | 0 | 0 | 0 | 0 |

**Thermal Testing**

Past durability testing done at NASA Glenn has primarily consisted of testing the prolonged functionality of packaged ICs at constant high-T attained under limited (usually 3 °C per minute) thermal heating and cooling rates. Important thermal cycle testing of electrically...
active NASA Glenn ICs remains to be accomplished as of this writing.

Post $T \geq 500 \, ^\circ C$ IC testing failure analysis has identified dielectric cracks initiating from the edge of a die or from wire-bonding mis-strikes [12]. To exclude packaging-related (extrinsic) stress and damage from these tests, individual “as-diced” unpackaged chips were placed onto a quartz plate and covered with hollow quartz cover (to protect chips from particle fallout) inside air-atmosphere ovens. The testing is therefore conducted without any electrical bias or grounding. Distinct sets of chips, wherein each distinct set was comprised of the sampling represented in Fig. 4, were each separately oven-tested in air ambient at 500 $^\circ C$, 600 $^\circ C$, 720 $^\circ C$, and 800 $^\circ C$ for 100-hour duration. A fresh (as-diced) bundle of 4-chip sets were then subjected to these same four temperatures for 200-hour duration. All the 100-hour and 200-hour tests employed maximum heating and cooling rates of 3 $^\circ C$/min. A third bundle of four as-diced 4-chip sets were “worst-case” tested for 10 thermal cycles between 50 $^\circ C$ and the same four peak temperatures, wherein each peak temperature was maintained for 10 hours each cycle. Thus, the total time at peak temperature for the 10 thermal cycles was 100 hours. However, heating and cooling rates for the thermal cycling were not explicitly limited, which resulted in nearly 20 $^\circ C$/min ramp-up rate and an exponential cooling rate to below 50 $^\circ C$ between each cycle. Fig. 3 compares the resulting temperature vs. time profile for a non-limited rate thermal cycle against the controlled ramp rates used for 100-hour and 200-hour experiments. 50 $^\circ C$ low temperature was selected to allow faster cycling (than passive oven cooling to room temperature) yet facilitate room-air water vapor reabsorption into the dielectric. 720 $^\circ C$ anneal temperature was chosen to match the 720 $^\circ C$ SiO$_2$ and Si$_3$N$_4$ dielectric layer deposition temperature.

Results

Table 1 summarizes the main overview experimental findings based on post-test optical microscope inspection numerical grading. As seen in the lower right grading legend, grade of 0 “Good” was given to chips remaining free of cracking (e.g., Fig. 4(d)), whereas grade of 3 “Ugly” was recorded for observation of dielectric areas peeling associated with severe cracking (e.g., Fig. 5(c)). The grading scale is intentionally skewed towards emphasizing failure and does not quantitatively distinguish the size of the failed areas on each chip. The pessimistic scale choice accounts for the harsh reality that crack-exposed TaSi$_2$ will oxidize and swell driving further crack propagation and oxidation over time that eventually results in trace open-circuit electrical failure [13,14]. It should also be noted that no distinguishable pattern was observed when we analyzed these results as a function chip position on the as-fabricated wafer.

The results of the two 10.2 chips are summarized in the left half of Table 1. It is important to note that 10.2 thermal cycling results are largely indistinguishable from the 10.2 constant temperature soak results. All 10.2 chips completely crack-failed by 720 $^\circ C$, except for one outlier at 800 $^\circ C$. Of the two 10.2 chip designs tested, the clock chips endured slightly better than the A to D chips. We speculate that this difference may arise from the chip layout differences, perhaps an effect of the power bus location. It should be noted that chips with 1 “Problem” grades could nevertheless have electrically operated for long duration at 500 $^\circ C$, depending upon specific crack location/extent unique to each chip not captured in the Table 1 results summary.

Wafer 11.1 chips (summarized in the upper right quarter of Table 1) did not fare as well as 10.2 chips, even though 10.2 and 11.1 have the same dielectric stack featuring only one nitride layer. It is suspected that the larger chip size of 11 (4.65 mm x 4.65 mm) compared to 10 (3.0 mm x 3.0 mm) is a contributing factor. While we cannot categorically rule out that the difference in TaSi$_2$ sputter deposition technique (pulsed DC for 10.2 vs. HiPIMS for 11.1), the majority of 11.1 cracks were not correlated with metal interconnect trace features that would be expected if metal film differences were responsible. Some post-test cracks on 11.1 were observed to start and stop in flat field areas in chips central regions void of edge effects, metal traces, or SiC topology.

In striking contrast to the discouraging 11.1 results, chips from wafer 11.2 (summarized in lower right of quarter of Table 1) exhibited no cracks below 800 $^\circ C$ aside from a single crack in noted the 600 $^\circ C$ 200-hour sample. Despite its larger die size, the 11.2 results are also substantially improved over the physically smaller 10.2 chips. The only process difference between 10.2 and 11.2 is this
lower Si$_3$N$_4$ layer. This experimental data indicates that the Si$_3$N$_4$ layer residing between Metal 1 and Metal 2 profoundly improved chip immunity to thermally driven dielectric cracking.

Due to the sheer number of post-testing images, illustrative chip images from only two key cases will be presented. The first case will be 10 thermal cycles to 500 °C to illustrate the differences between the numerical grades 0, 1, and 2 presented in Table 1. The second case will 10 thermal cycles to 720 °C because it compellingly illustrates the superior durability obtained on Wafer 11.2. All images presented below in Fig. 4 and Fig. 5 were recorded using white-balanced camera calibration so that field-region color differences between versions are as-shown. The extra Si$_3$N$_4$ layer in 11.2 as well as field implant dose difference are believed responsible for field-region color change. No field-region color change was apparent when directly comparing pre-test and post-test images of the same chip for 11.2.

**Results After 10 Cycles to 500 °C**

Fig. 4 shows the optical images of the 10 cycles at 500 °C tests (with 10-hour hold at 500 °C each cycle). Parts (a-d) of Fig. 4 are presented at the same magnification scale in order to emphasize the chip size difference, whereas higher magnifications used for parts (e-g) are denoted with individual scale annotations. The arrow on Fig. 4(e) denotes the single crack found on the A to D chip across the power bus. Since there was no discoloration associated with the crack, the resulting grade of 1
was assigned. Cracks were often observed on such relatively long and large 10.2 Metal 1 power bus lines with acute angle features. Likewise, the non-discolored crack highlighted by the white arrow in Fig. 4(f) (also running across Metal 1 power bus) also resulted in a grade of 1 for the 10.2 ÷2/÷4 clock chip. The multiple arrows in Fig. 4(g) illustrate some of the multiple cracks observed for 11.1, including some examples where discoloration around the crack is readily apparent. This 11.1 chip therefore received a grade of 2. The single arrow in Fig 4(d) points to a processing blemish in the SiC itself that was present and documented prior to the testing. No cracks whatsoever were found on this 11.2 chip after the 500 °C thermal cycling, which resulted in a score of 0 “Good” for this chip.

Results After 10 cycles to 720 °C

Images recorded after 10 cycles to 720 °C (with 10-hour hold at 720 °C each cycle) are presented in Fig. 5. In contrast to Fig. 4 (a-d), the lower magnification images Fig 5(a-c) of 10.2 and 11.1 clearly show catastrophic damage corresponding to a grade of 3. Where dielectric has peeled or cracked, discoloration is readily evident, and blackening occurs where exposed TaSi2 has extensively oxidized. Fig. 4(b) shows that some chip regions are more heavily damaged than others. With metals surrounding all bonding pads blackened and substantial areas of power bus traces missing, the Fig. 5(c) 11.1 chip clearly exhibits significantly more damage than 10.2. Remarkably, the 11.2 chip in Fig. 5(d) exhibited no dielectric cracks in the electrically active circuit area. The feature denoted by the arrow in (d) is a SiC mesa-etch defect documented prior to the test. Parts (e), (f) (g) are corresponding higher-magnification close-ups of areas of interest as indicated by blue dashed box annotations on the lower-magnification images (see text).
5(d) exhibits no observable damage throughout all active circuit and bonding pad regions. As shown in Fig. 5(g) the only damage observed on 11.2 was confined to Metal 1 “fence” pattern that separates the dicing path from the rest of the chip. Because the SiC and dielectrics in field regions are transparent, one should notice that the backside metal has only a slight region of discoloration confined to small areas of lower left corners in Fig. 5(d) and Fig. 5(g). Most of the backside metal of 11.1 in Fig. 5(c) has peeled leaving circular patterns of remaining metal. About 20% of the 10.2 backside metal areas appear peeled in Fig. 5(a) and Fig. 5(b). Fig. 5(e) clearly illustrates dielectric cracks that start/end at the diced edge of the die and travel considerable distance across the chip before hitting a metal trace. Fig. 5(e) also shows an example of interconnect damage and discoloration associated with an overlying dielectric crack. Fig. 5(f) is a higher-magnification photo of the damage difference observed between the left side and right side of the 10.2 clock.

Summary Discussion
The dominant attribute that distinguishes 11.2 from the less-durable 10.2 and 11.1 chips is the addition of a lower layer of stoichiometric Si$_3$N$_4$ between Metal 1 and Metal 2. Note that the Si$_3$N$_4$ layer is only 63 nm thick, less than 1% of the total combined dielectric stack thickness. If the metal interconnect crack/void failure over topology shown in Fig. 2 can be remedied, this study suggests that it is plausible to make SiC ICs that can operate at 720 °C for at least hundreds of hours. These same improvements should also increase the reliability and durability of SiC ICs operating at 450-500 °C [1-3].

References