

NASA

STUDY OF A HIGH VOLTAGE ION ENGINE POWER SUPPLY

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by

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Chapter 1

INTRODUCTION

The design constraints for space power converters differ from those of terrestrial converters in several important ways: (1) low mass is important because of the high cost of boosting it into space, and (2) high power efficiency is even more important because of the incremental mass in the heat removal system associated with a low efficiency converter. High switching frequency is only useful to the extent that it allows weight reduction in the complete system comprising the switching converter and its heat removal system.

This study included a survey of various DC/DC converter topologies in order to select the most appropriate ones for a 1.8 kW ion engine power supply. This supply actually consists of three converters that provide the following power sources:

1. A 1.8 kW source with an output of 500 - 1350 V.dc.
2. A 150-250 V.dc source that delivers 20 m.a. steady state and a 1 amp surge current.
3. A ± 15 V.dc housekeeping supply.

In addition to selecting the topologies for these converters, their implementation often required a choice from several different technical options. A number of subtle problems also were encountered, and these frequently determined which technology was used. The more important choices and problems are discussed in the next chapter, and it is hoped that some of this information will be useful in the design of power supplies for future ion thrusters.

Chapter 2

TECHNOLOGY SURVEY

Several factors determined the choice of the converter for the 1.8 kW source:

1. DC isolation between input and output
2. Voltage transformation ratio
3. Input voltage
4. Power level
5. Component limitations
6. Efficiency
7. Low mass
8. Reliability

The need for DC isolation obviously restricts the choice to a topology with a transformer. Actually, the high voltage transformation ratio (which has a maximum value of 1350/80) also would dictate this choice. The next basic decision is to select a circuit from the wide variety of forced switching and resonant topologies. The low switching loss of FETs virtually eliminates the need for relatively complex resonant circuits such as the series and parallel loaded types. V_{DS} limitations of FETs then point to the full bridge topology. Finally, one must decide between diagonal and phase-shift control. Diagonal is the simplest, but phase-shift readily allows the implementation of zero voltage switching (ZVS) over the upper end of the load range. This reduces both switching loss and snubber requirements for the FETs.

The next choice is between,

1. Current mode control (CMC)
2. Average current mode control (ACMC)
3. Voltage mode control (VMC)

First, one should be aware that all bridge and push-pull circuits must guard against momentary flux imbalances that can lead to transformer saturation. If this happens, the transformer primary appears as a short circuit, and if the circuit is unprotected the results are usually catastrophic.

One possibility is to place a large capacitor in series with the primary, but at higher levels this capacitor is subject to serious heating, mass and efficiency problems. CMC is also a popular solution to this problem, and it provides wide bandwidth which helps improve the transient response. However, CMC demands a sanitized replica of the load current waveform (e.g., minus turn-on transients and EMI) for the control circuit, and obtaining this can be tedious. CMC is certainly do-able, but the difficulty in obtaining waveform replica at higher power levels motivates the search for a simpler approach.

ACMC was considered, but to provide flux balance this also requires a signal that responds to the instantaneous current. This approach was investigated, but it was eventually abandoned because of transients and EMI problems.

Because of the implementation complexities of CMC and ACMC, it was decided to investigate VMC for this application. VMC alone is always vulnerable to transformer saturation, but the circuit was altered to avoid this, and the resulting system appears to be less sensitive to transients and EMI than either CMC or ACMC. First of all, for steady

state operation there are some factors that help to prevent transformer saturation. To explain this, it should be recognized that the conduction time periods and parasitic voltage drops in the two halves of the circuit are always slightly imbalanced. This means that the transformer core will operate at one end of its BH loop, and one half cycle will be on the verge of saturation. At the end of this half cycle, the magnetizing current will increase slightly as the end of the BH loop is approached, and the increasing iR drop will decrease the voltage applied to the winding. It is this iR drop that forces the flux to ultimately balance for the two half cycles, and the core will then operate on a steady state minor BH loop. This is perfectly acceptable as long as the increased magnetizing current on the one half cycle doesn't become excessive. FETs are very helpful in this respect because they are resistive and have positive temperature coefficients. They also minimize conduction time imbalances between the two half cycles because their switching times are very small, and thus any time imbalance is very very small compared to a half period. If the current saturation current on one half cycle is still too high, it can often be decreased to an acceptable level by increasing the gap in the transformer core. This increases the magnetizing current so the necessary iR increase can be achieved at a lower saturation level. In this particular application, acceptable steady state operation was achieved without increasing the transformer gap.

Although features such as parasitic R and core gaps can provide satisfactory steady state operation, they cannot guarantee the avoidance of saturation during transient conditions. Thus saturation may still randomly occur during situations such as start-up or output faults. To avoid FET failures during these conditions an active circuit must be used to protect the FETs. In this case a current sensor and controller was used to detect

excessive primary currents, turn-off the circuit, and then use a soft re-start. In spite of this extra circuitry, the resulting VMC system was judged to be easier to implement than a CMC or an ACMC system. As noted earlier, stabilization of VMC requires a lower bandwidth than CMC or ACMC, and thus a slower transient response results. The transient response was still considered to be adequate for this application however, and this was not judged to be a serious limitation.

The original controller for the 1.8 kW converter used the UC3875 control chip. Although simple to implement, this chip had very poor EMI immunity and was quickly abandoned. A second controller was implemented with discrete I.C.'s and used a control strategy very similar to that in the 3875. No serious EMI problems were encountered with this new controller.

Chapter 3

THEORY OF OPERATION

A block diagram of the complete system is shown in Dwg. A. The system provides the following outputs:

1. +1350 V.dc, 1.8 kW. (HV Output)
2. -150 to -250 V.dc, 250 W. for 100 m.s. (LV Output)

Short circuit protection is provided for faults between either output and COM or between the two outputs. In the event of a fault, this protection circuitry de-energizes the system as specified by NASA, and it must be re-started manually. The system also provides its own ± 15 V.dc housekeeping power supply to avoid grounding limitations associated with externally available supplies.

The HV power circuit in Dwg. B employs three parallel 300 volt FETs in each leg of a full wave bridge. A layered interconnect structure is used on the primary in order to minimize parasitic inductance.

The transformers used in most bridge and push-pull converters invariably have leakage inductances, $L\ell$, that are larger than desired. Thus the usual design strategy should minimize $L\ell$, and that was done in this case for the HV transformer. This was achieved by using a 3 turn foil winding on one leg of a UU core, wrapping this with a layer of insulation and then winding the secondary in single layer sectors directly on top of the insulation. This achieved an $L\ell = 0.51\mu\text{H}$ when measured on the primary. Unfortunately this was actually too low and resulted in an excessive current transient at

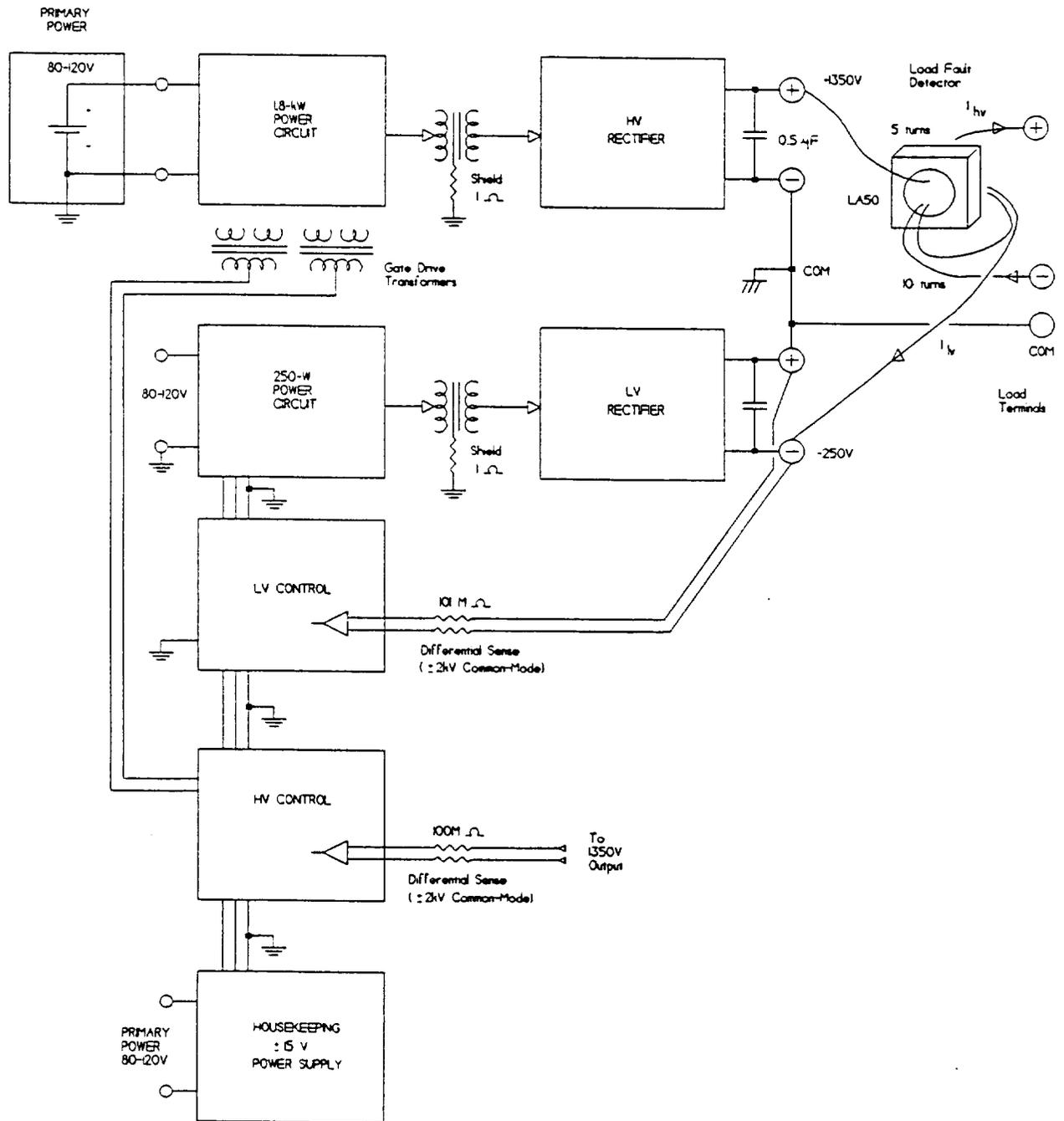
turn-on. To reduce this transient to an acceptable level, it was necessary to add an external inductance of $2\mu\text{H}$ in series with the primary.

If the transformer was re-designed, it would be advantageous to use a more compact arrangement, perhaps with more turns of multi-layer windings on a smaller core. This should reduce the weight and increase $L\ell$ to the desired value. The switching frequency of 60 kHz was selected primarily to provide a sufficiently low flux density in the transformer core. To accommodate the 1350 V.dc output at this frequency, it was necessary to use 5 rectifier bridges connected in series as shown in Dwg. B. Even with 1000 volt diodes, switching voltage transients required the use of substantial snubbers for these rectifiers. It was originally thought that this problem would be alleviated by use of the RHRU150100 diode because of its low t_{rr} and soft recovery characteristic. However, this diode is designed for currents well in excess of the 1.8 A.dc maximum load current, and it has a large wafer with a high junction capacitance. this produced both current and voltage transients that were excessive and could not be reduced to satisfactory levels with reasonable snubbers. thus it was necessary to resort to the BYT08P diode with its lower junction capacitance even though it does not have soft recovery.

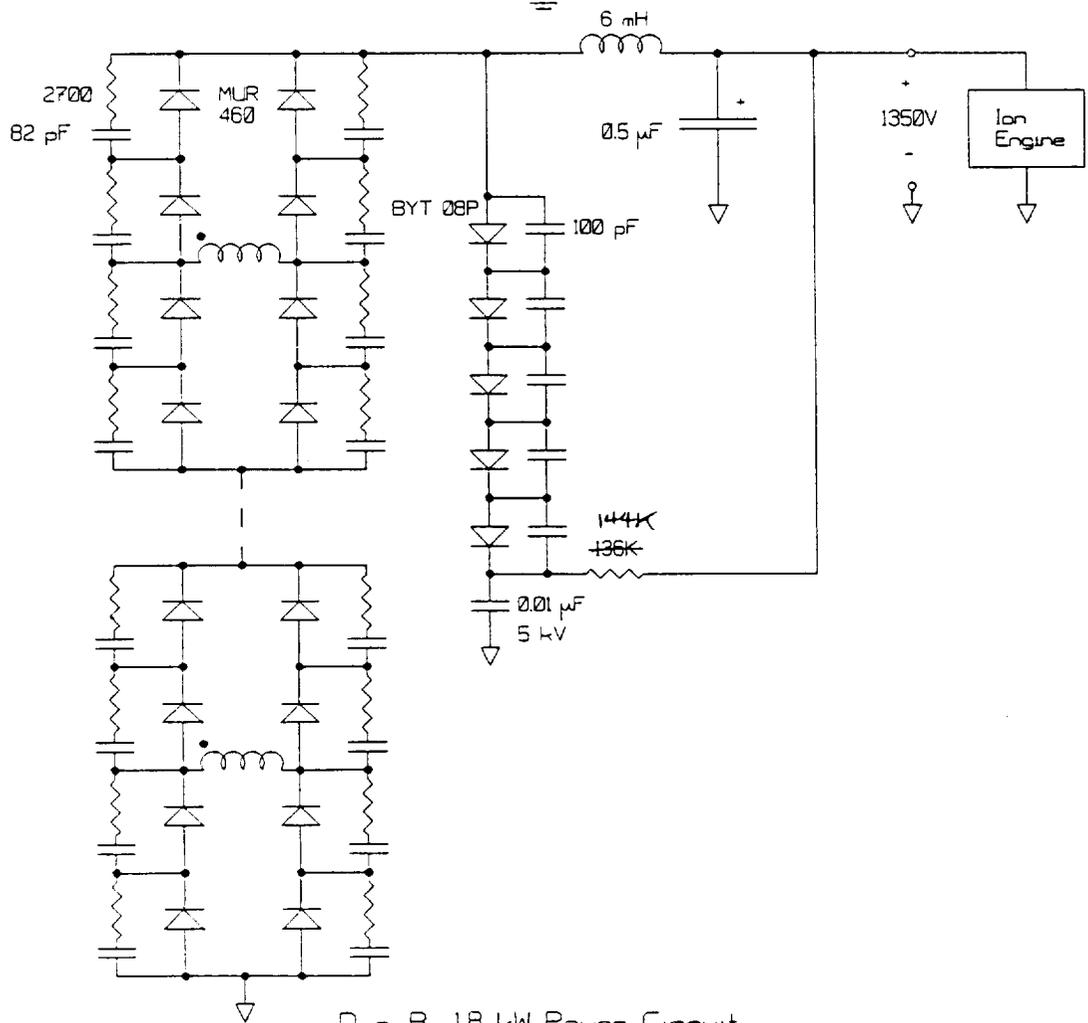
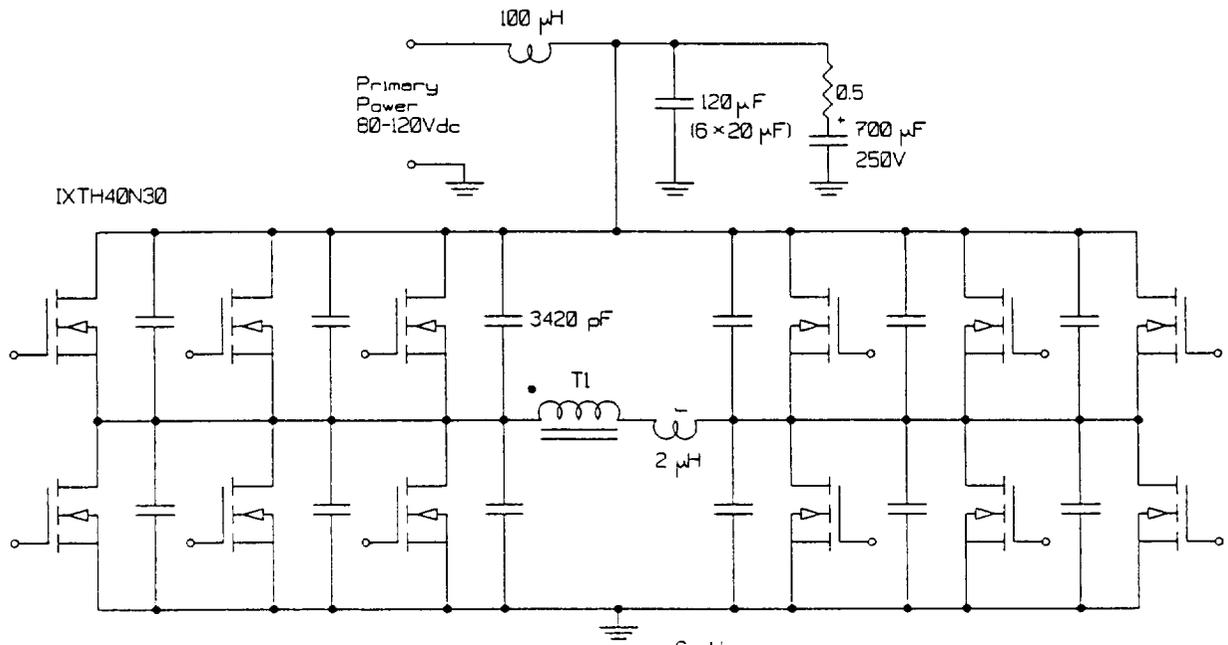
Another feature of interest is the output voltage sensing circuit shown in detail in Dwg. D for the HV converter. Strictly speaking, this circuit does not provide complete DC isolation between the input and output ground. However, it does provide $1000\text{M}\Omega$ of isolation, and this was considered adequate. This design provides a considerable simplification over other alternatives such as optical or transformer isolation.

The LV converter in Dwg. G has a maximum steady state load of only 5W., and this could be derived from an extremely small converter. However, it also has to supply a 1 amp surge for 100 m.s. with less than a 50% voltage droop. If a very small converter was used, this surge specification would require the use of an extremely large output capacitor. Instead of supplying this pulse from a capacitor, it was determined that considerable weight and volume could be saved by designing the converter itself to supply a 1 amp surge for 100 m.s. Although this necessitates much larger semiconductors in the converter, the complete weight and volume are much less than the large capacitor version. the converter now has a 100 m.s. rating of 250W., but this is still within the range where simpler topologies are effective. Therefore a relatively simple forward converter was selected for this circuit.

Although a $\pm V$.dc source is available externally, the ground for this source cannot be connected to either the input ground or the output ground of the ion engine power supply. Therefore, it was decided to provide the dedicated $\pm 15 V$.dc housekeeping source in Dwg. I whose ground would be connected to the input ground. Because of the low power level, a simple topology is also adequate for these sources, so a forward converter similar to that for the LV source was selected.

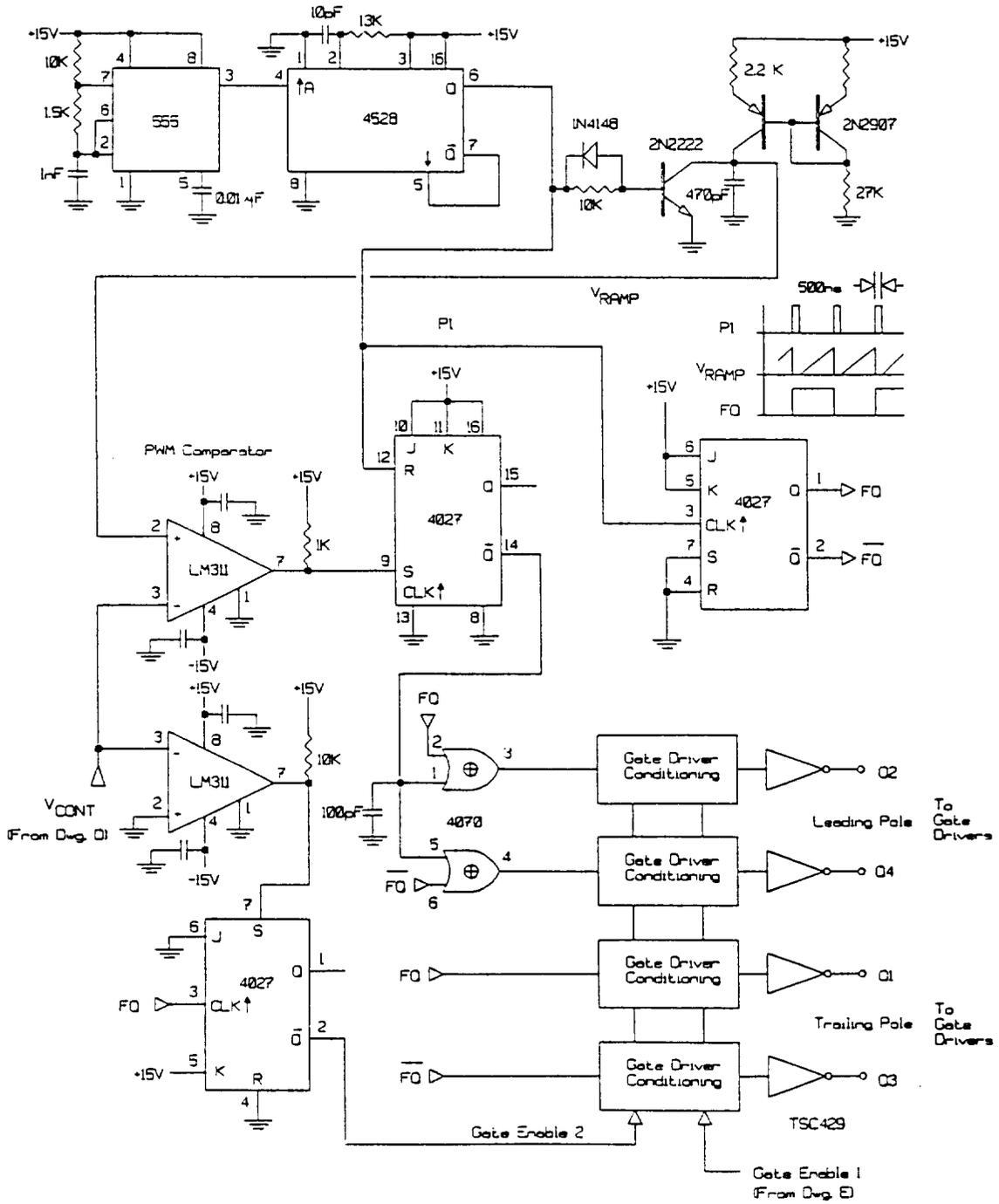


Dwg. A System Block Diagram - Grounding and Isolation

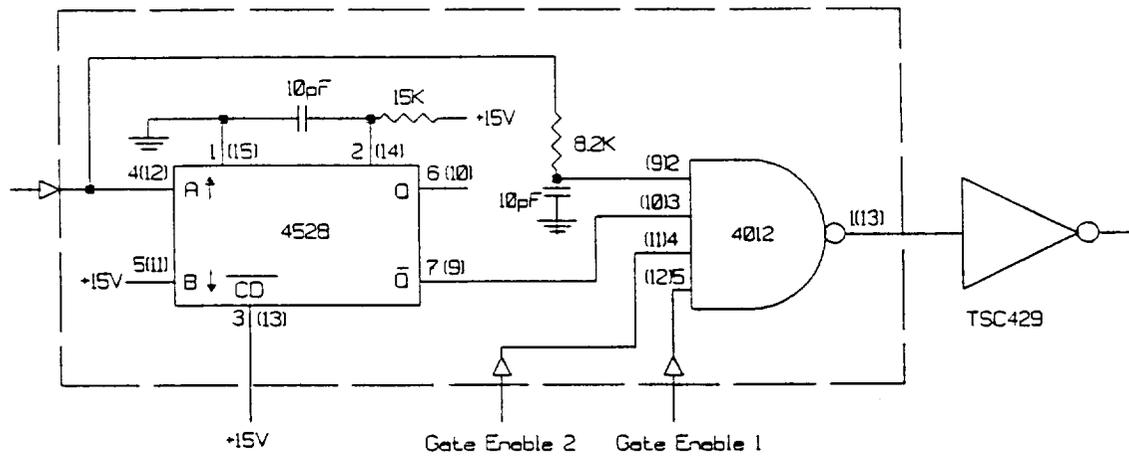


B1
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B5

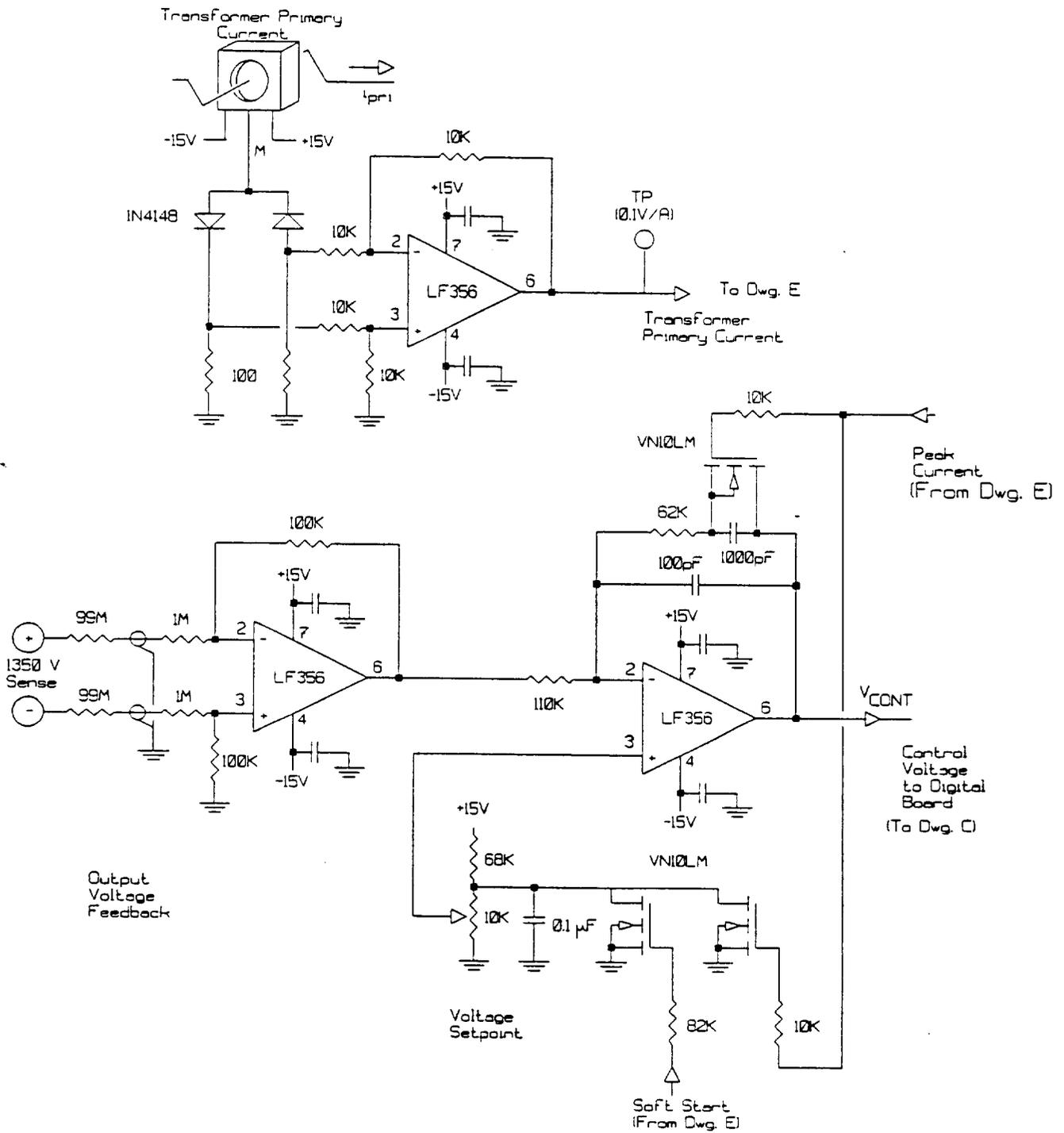
Dwg. B 1.8 kW Power Circuit



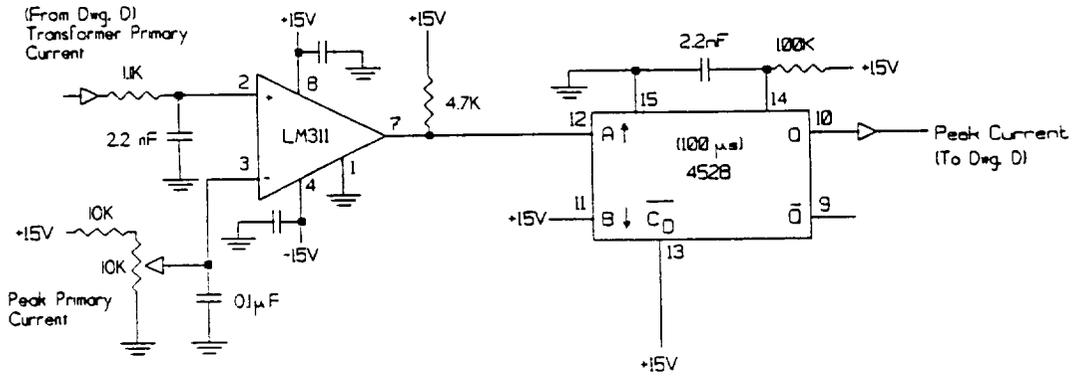
Dwg. C IV Control - Digital Circuitry



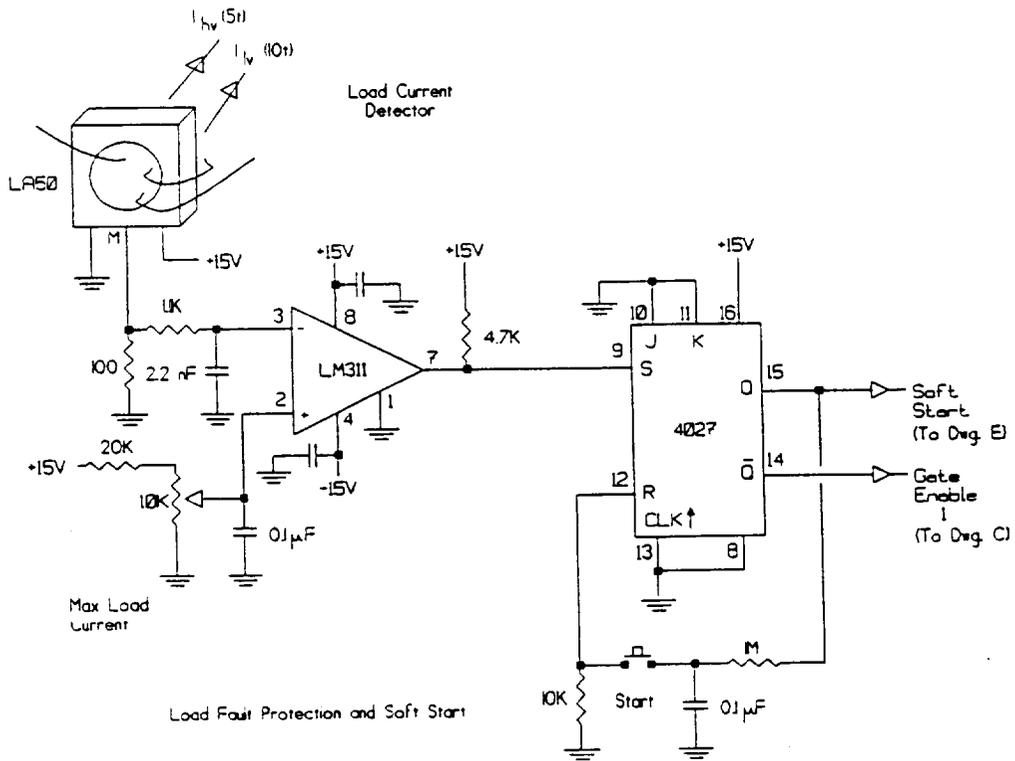
Dwg. C (Detail) Gate Driver Conditioning Circuit



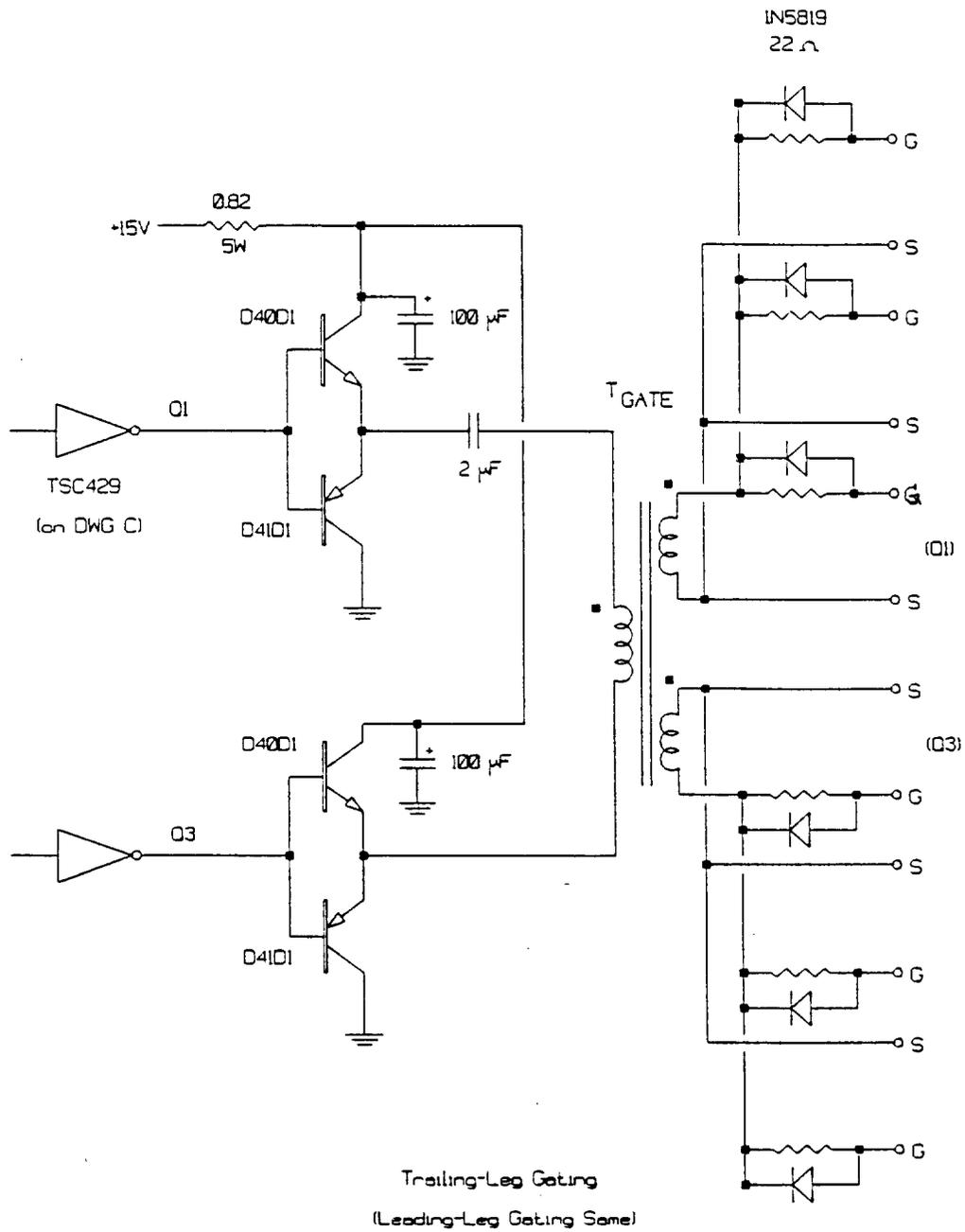
Dwg. D HV Control - Analog Circuitry



Primary Peak Current Detector



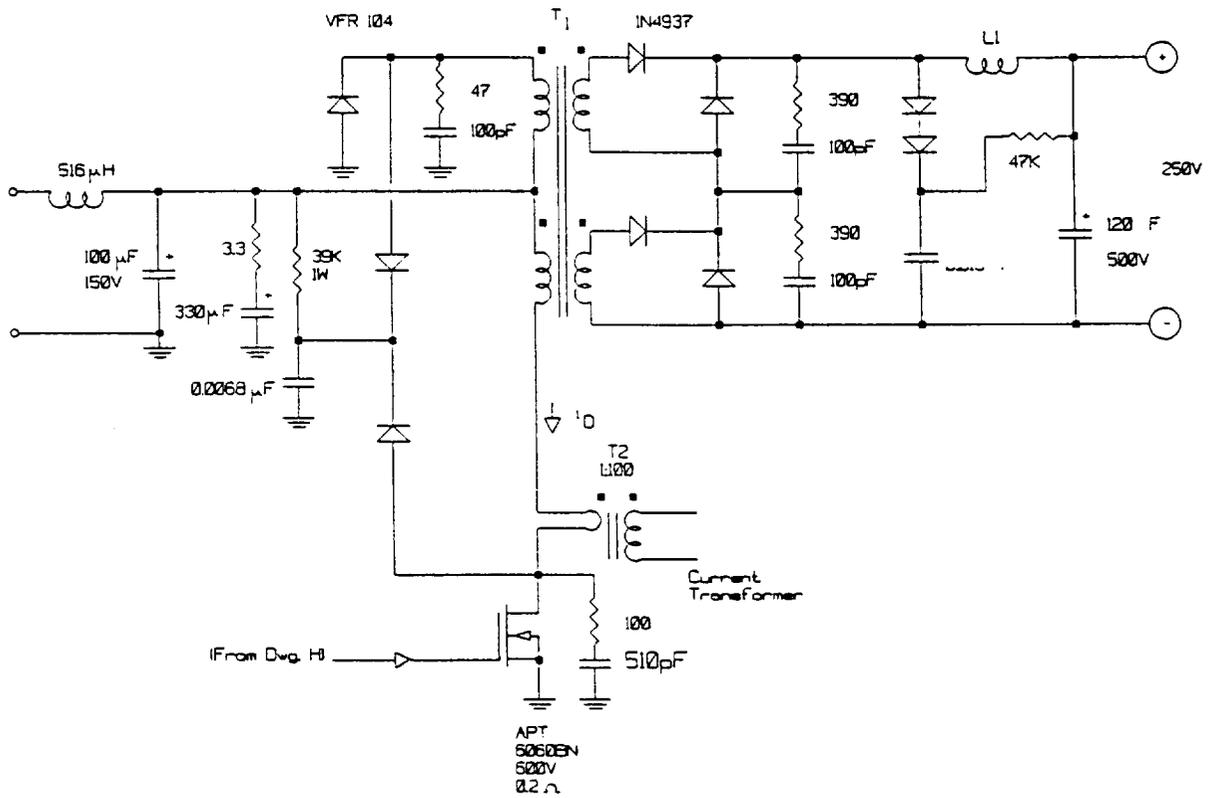
Dwg. E HV Control - Soft Start and Protection



T_{GATE} Data

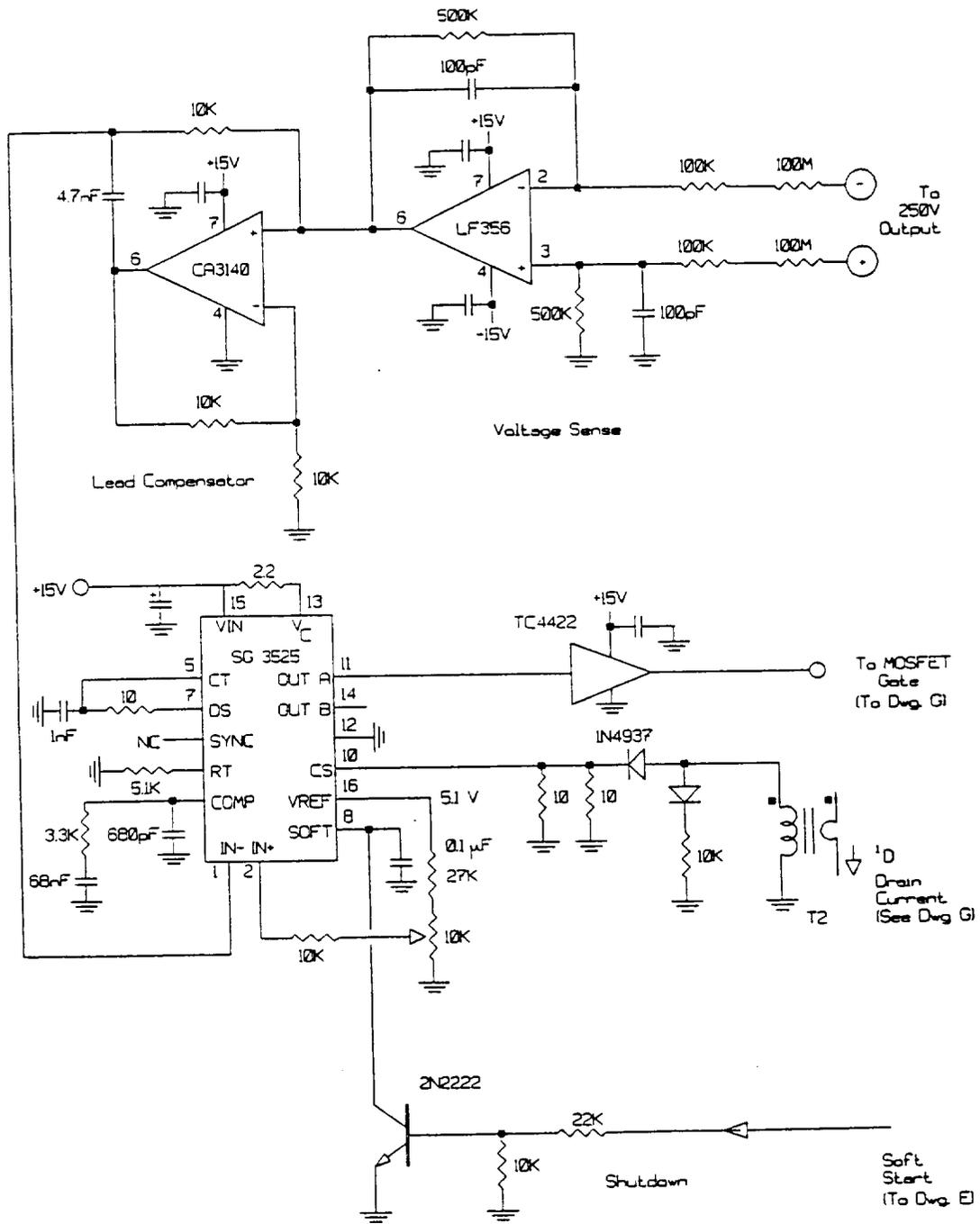
3622 pot core
 5 turns trifilar
 teflon insulated hookup wire

Dwg. F HV Gate Drivers

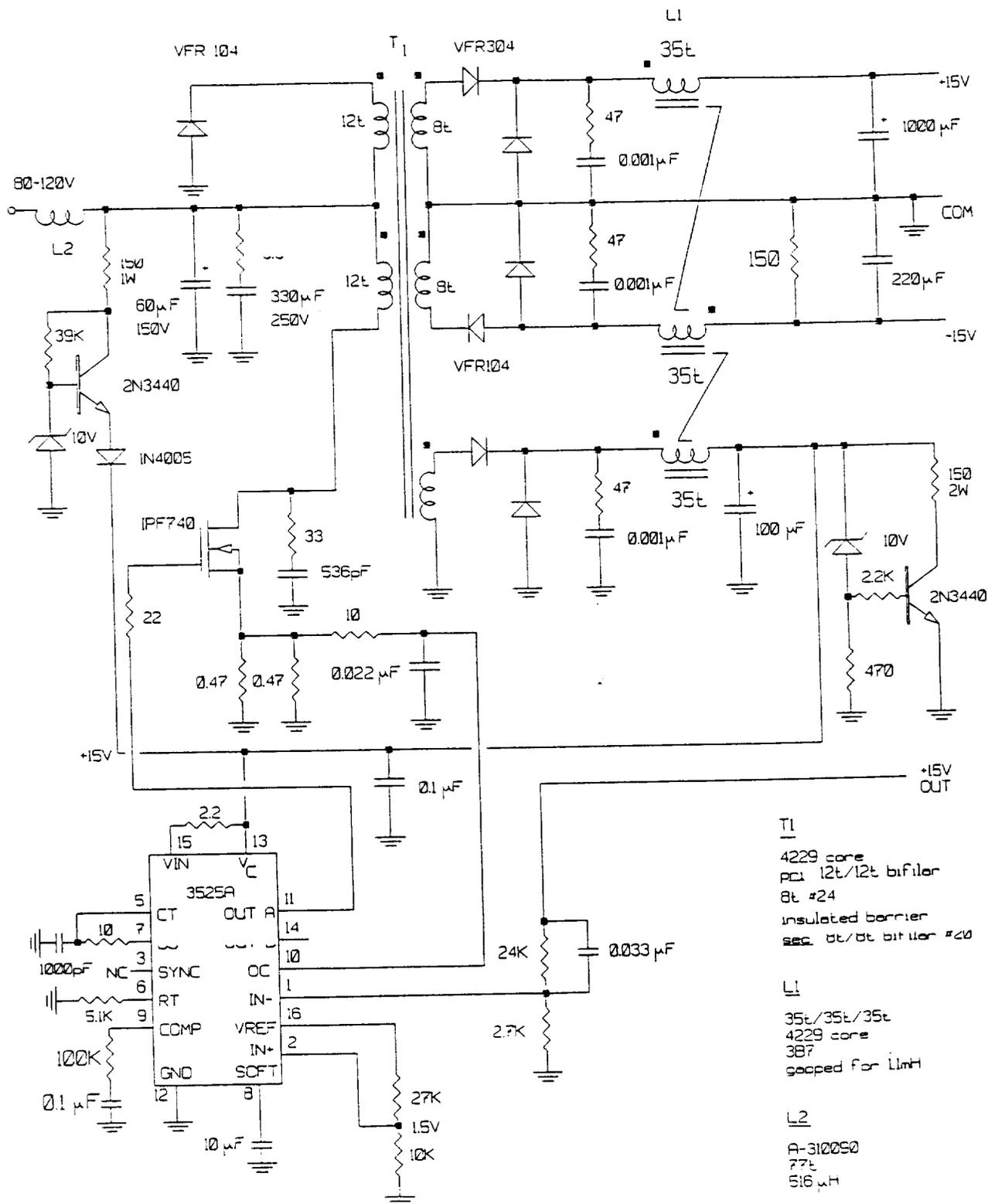


T1 Data	T2 Data	L1 Data
Primary: 10t + 10t	Primary: 1t	99 t
Secondary: 35t + 35t	Secondary: 100t	T106-26 Core
Core: EC-52	Core: 3019 3B7	

Dwg. G LV Power Circuit



Dwg. H LV Control Circuit



Dwg. I Housekeeping Supply

Chapter 4

EXPERIMENTAL RESULTS

The measured experimental performance of the ion-engine converter was reported briefly in [1]. A copy of this paper is included in Appendix A. A more complete report is given in this chapter.

Diode Selection

The output rectifiers were identified early in the project as an important contributor to the losses, primarily because of the need for heavy snubbing of the output rectifiers to avoid large reverse voltages at high line. A lossless snubber would aid in lowering the snubbing loss, but was deemed unnecessarily complex for this power level. The development effort was expended on finding the best possible diodes for the rectifier. In this context, best was defined as the diodes which could be snubbed to an acceptable overshoot voltage with the lowest overall losses.

A workable choice was found in the BYT 08P diode. This device is made by Temic (formerly Siliconix) and is rated at 8 A and 1000 V, with a 120 ns reverse-recovery time. Five bridge rectifier sections, each associated with a separate transformer winding and using four diodes, were used with the BYT 08P diodes. Additional improvement was obtained in the final packaged version of the power converter by changing the output rectifiers to Motorola MUR460s, rated at 4 A and 600 V, with a reverse-recovery time of 75 ns and a CJO of about 150 pF. This required five bridge rectifier sections, each with a separate transformer winding

and eight diodes, series connected in groups of two. This rectifier arrangement is shown in Dwg. B. The damping snubbers were distributed so that they would also function as voltage equalizers for the diodes. Experimental work with 1N6628s showed that they would produce results nearly equal to the MUR460s.

A typical dc-side voltage for one bridge section of the output rectifier is shown in Fig. 1. This scope waveform was taken at high line ($V_{in} = 120 \text{ V}$) and a load of 1.51 A at 1100 V. The peak voltage of 600 V appearing under these conditions is distributed across two MUR460 diodes. The character of the waveshape appearing here is invariant for high and low line conditions: the amplitude and duty factor change with line and load conditions, but the lightly-damped ringing, with some clipping of the first voltage overshoot, appears under a wide range of conditions. The total rectifier output voltage (before the filter) and the dc-side voltages of the individual bridges were observed under a variety of conditions. They were found to indicate peak voltages at the individual bridges within 20% of the expected values. The initial clipping of the transient voltage in Fig. 1 is caused by the voltage clamp composed of five BYT 08Ps, the 0.01 μF capacitor and the 144 K resistor (see Dwg. B). This clamp features partial energy recovery by virtue of the fact that the resistor bleeds charge from the capacitor to the output terminal. Experimentally, it was possible to operate the converter with only the clamp and no damping elements on the individual bridges, or to use only damping elements (the series R-C networks) on the bridges and no clamp. However, the lowest overall losses while meeting the goal of a conservative diode reverse voltage was met with the combination of clamping and damping shown in Dwg. B. Observation of the diode currents and voltages also showed no evidence of significant reverse-recovery problems: the observed ringing waveforms can be

Tek



Cursors

Window1

Def Wfm

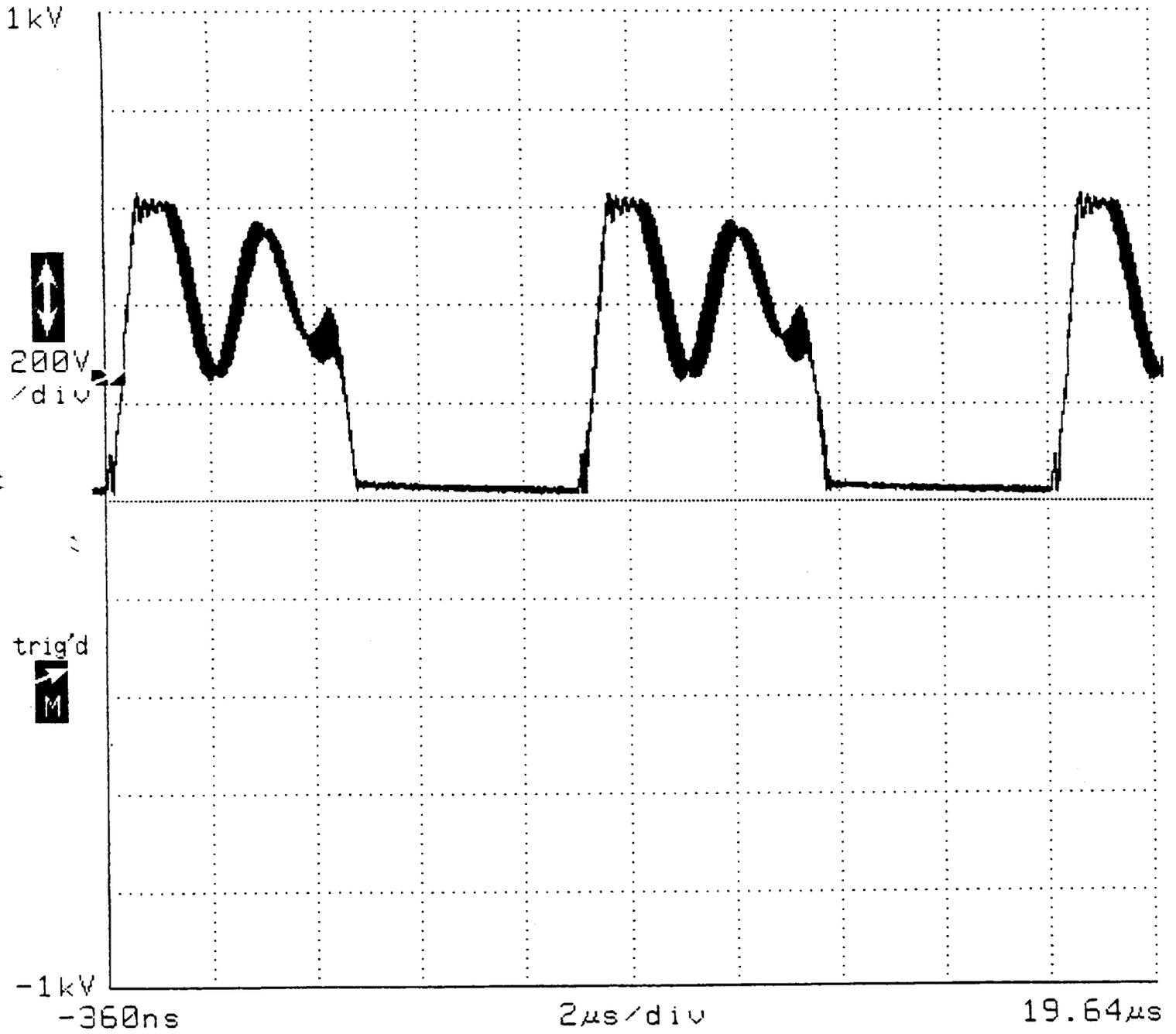


Fig. 1 DC-side voltage for one bridge section of the HV rectifier.

Waveform: V_{DC} at 200 V/div

Timebase: 2 μ s/div

explained solely in terms of the diode junction capacitances. The criteria used to search for rectifier diodes were therefore (1) low junction capacitance, with (2) adequate current rating and (3) high voltage rating.

Power Efficiency

The measured efficiencies of the 1.8 kW high-voltage converter under several conditions are given in Table 1. The efficiency of operation at high line was generally found to be lower due to the rapid increase in losses in the rectifier dampers and clamp. System no-load performance is summarized in Table 2, which includes losses in the housekeeping power supplies and the low-voltage converter.

Table 1
Measured Efficiency of the 1.8 kW High-Voltage Converter

	Input Voltage/ Input Current	Output Voltage/ Output Current	Output Power/ Efficiency
Low Line/ Full Load	80 V 23.6 A	1106 V 1.53 A	1687 W 92.2%
High Line/ Full Load	120 V 16.1 A	1106 V 1.53 A	1687 W 89.7%
Low Line/ Maximum Output	80 V 25.0 A	1322 V 1.37 A	1816 W 93.3%
Low Line/ Half Load	80 V 12.0 A	908 V 0.94 A	853 W 90.7%

Table 2

Measured System No-Load Power Consumption

Input Voltage	Input Power	LV Output Voltage	HV Output Voltage	System Status
80 V	12.8 W	250 V	1350 V	Operating at No Load
120 V	12.0 W	250 V	1350 V	
80 V	9.6 W	-	-	Standby (Housekeeping Active)
120 V	10.8 W	-	-	

Loss Breakdown

The losses in the 1.8 kW high-voltage converter were carefully measured under near full-load (1106 V at 1.525 A) at high line and low line. For these two cases, the losses were broken down among the various components of the converter as carefully as possible, using direct measurements in some cases, and calculation or simulation in others to estimate the corresponding losses. The results are summarized in the following.

Table 3 lists the test results, giving the directly-measured total loss, along with the estimated loss for each component. The total loss was measured by subtracting the measured output power from the measured input power, using dc instruments calibrated at levels near to

the measured values. The corresponding measured power efficiencies are also listed in this column.

MOSFET losses were estimated through heatsink temperature-rise matching. The converter was run until thermal steady-state was reached, and the heatsink temperature rise was recorded. The MOSFETS were then diode connected and heated using a dc supply. The power level was adjusted to produce a matching temperature rise; the power level was then easily measured. The measured heatsink temperature is also listed in the third column of Table 3. It may be noted that the higher power produced the lower temperature because this test was done on a day having a lower ambient temperature: temperature rise was actually matched in this procedure. This method was used to avoid the uncertainties in accounting for conduction and switching losses in the MOSFETs, inclusion of the losses in the MOSFET anti-parallel diodes, and change of $r_{DS(on)}$ with temperature.

Table 3

Measured/Estimated Losses by Component Under Full-Load Conditions

Test Conditions	Total Loss (Directly Measured)	MOSFET Loss	HV Clamp Resistor	HV Rectifier & Damper	Housekeeping Losses	Power Transf.	Sum of Individual Losses
Low Line Input: 79.3 V, 23.1 A Output: 1106 V, 1.525 A	142 W $\eta=92.2\%$	75 W ($T_{SINK}=74^{\circ}C$)	9.9 W	31.6 W	17.8 W	7 W (core) 24 W (Cu)	165 W
High Line Input: 119.8 V, 15.7 A Output: 1106 V, 1.525 A	194 W $\eta=89.7\%$	85 W ($T_{SINK}=70^{\circ}C$)	33.4 W	38 W	19.0 W	7 W (core) 11 W (Cu)	193 W

The losses in the high-voltage clamp resistor (marked 144 K on Dwg. B) were easily found by direct measurement of the dc voltage on the resistor. The voltage ripple appearing on both the output and clamp capacitors was deemed minimal.

The losses in the high-voltage rectifier diodes and their associated dampers were virtually impossible to directly measure, because they occur in 40 individual diodes and 40 individual damper resistors. The voltages and currents involved contain large switching-frequency content and are superimposed upon large common-mode voltages. In addition, it appeared that attempting to insert measuring equipment in the rectifier would alter the operation of the converter enough to affect the accuracy of any attempted power measurements through the stray capacitance added by these connections. Therefore, a computer simulation using PSpice was used to estimate the power losses in the rectifier. This was done by simulating a SPICE model of one bridge rectifier section (having 8 diodes) with its corresponding transformer secondary. The clamping circuit was modeled as an ideal voltage source, apportioned to one-fifth of its measured value, in series with a diode. The transformer was modeled as a transient voltage source, equal to the observed primary waveform reflected to the secondary, behind an internal inductance equal to the measured leakage inductance for one secondary winding. The SPICE diode model included its capacitance, initially estimated from the data sheet. The transient SPICE simulation was done parametrically, changing the diode junction capacitance until the overshoot and ringing voltages observed in the simulation matched those observed experimentally. The static SPICE diode parameter "N" (the emission coefficient) was then adjusted such that the simulation showed the same diode forward voltage drop as that predicted by the diode data sheet. At this point, SPICE was called upon for the integral of the input and output i-v products over one

switching period, thus allowing the estimation of the total rectifier losses, including switching, conduction and damping elements. The results of this simulation were used to produce the entries in the fifth column of Table 3.

The housekeeping losses listed in the sixth column of Table 3 include all power expended by the low-voltage logic power supplies and the low-voltage output (250 V), running unloaded. This loss was measured directly using dc instruments.

The power transformer losses were estimated in two parts: the core losses and the copper losses. The core losses were calculated using the data sheet for the core material. Core losses were also measured directly through an open-circuit test using a square wave with an amplitude and frequency equivalent to that of the converter. There was excellent agreement between these two methods. The copper losses were measured experimentally through a short-circuit test using a sine wave of the correct frequency and rms value equivalent to that of the complex current waveform in the converter. The sinusoidal test current was generated using a low-power source and series-resonating the leakage inductance of the transformer under test. In both cases the losses were measured using the digital oscilloscope.

The right-hand column of Table 3 shows the sum of the individually-measured losses. The agreement between the sum of the individually-measured losses and the directly-measured loss is considered good.

Transient Performance

The transient performance of the HV power supply is documented in Figs. 2 and 3: Fig. 2 is for a 100- Ω fault between the +1100-V and -250-V terminals, and Fig. 3 is for a dead short

between these same terminals. Fig. 2 is a set of waveforms acquired while operating at full load on a 80-V line voltage. The upper waveform in this figure is a logic signal indicating that the current sensor protecting the load has detected the inception of the fault current. The next waveform below this in Fig. 2 is the -250-V output, at 200 V/div, center reference. The lower pair of waveforms are the +1100-V output voltage, and the HV output filter inductor current, at 1 kV/div and 2 A/div, respectively. It can be seen that the fault current is sufficient to drain the output capacitors on both the HV and LV outputs in about 30 ms. The the converter is shut down at the rising edge of the fault detect signal without any evidence of transient over-current on the HV output.

Fig. 3 is a set of waveforms acquired while operating at full load on a 120-V line voltage. The fault in this case is a dead short. Again, the upper waveform is the logic signal indicating detection of the fault. The waveform below that is the LV output voltage at 200 V/div. The lower pair of waveforms are the HV output voltage at 1 kV/div, and HV output filter inductor current at 2 A/div. Several observations may be made from these waveforms. The apparent ripple frequency in the filter inductor current is about 110 Hz, while the actual ripple frequency is 110 kHz. This illustrates a hazard of the digital sampling oscilloscope: the sampling rate available under the acquisition conditions used was too low to prevent aliasing. However, additional investigation showed that the peak-to-peak value of current ripple apparent in this waveform was the actual value, and this aliasing effect does not impair the utility of these results.

Another observation is that the HV output voltage collapses almost immediately, while the LV output voltage holds up for about 4 ms with little effect, and then collapses abruptly. This phenomenon is explained by the fact that the LV output has a large filter capacitor (120 μ F),

and the HV output has a small filter capacitor (0.5 μ F). The energy stored in the HV output capacitor is released quickly, leaving the HV inductor to support the voltage appearing on the LV capacitor (about 250 V). The flux in the HV filter inductor ramps up to its saturation value after about 4 ms, and then the energy stored in the LV capacitor is rapidly discharged through the faulted load, the HV filter inductor, and the HV rectifier diodes. The peak discharge current through this path is about 20 A. This value is within the capabilities of the HV diodes used; however, the phenomenon illustrates an additional difficulty which would be encountered if one attempted to design for the LV load-current step response by using a small converter and a very large capacitor. It might be anticipated that the peak value of this discharge current would become unmanageable if a much larger LV filter capacitor were used.

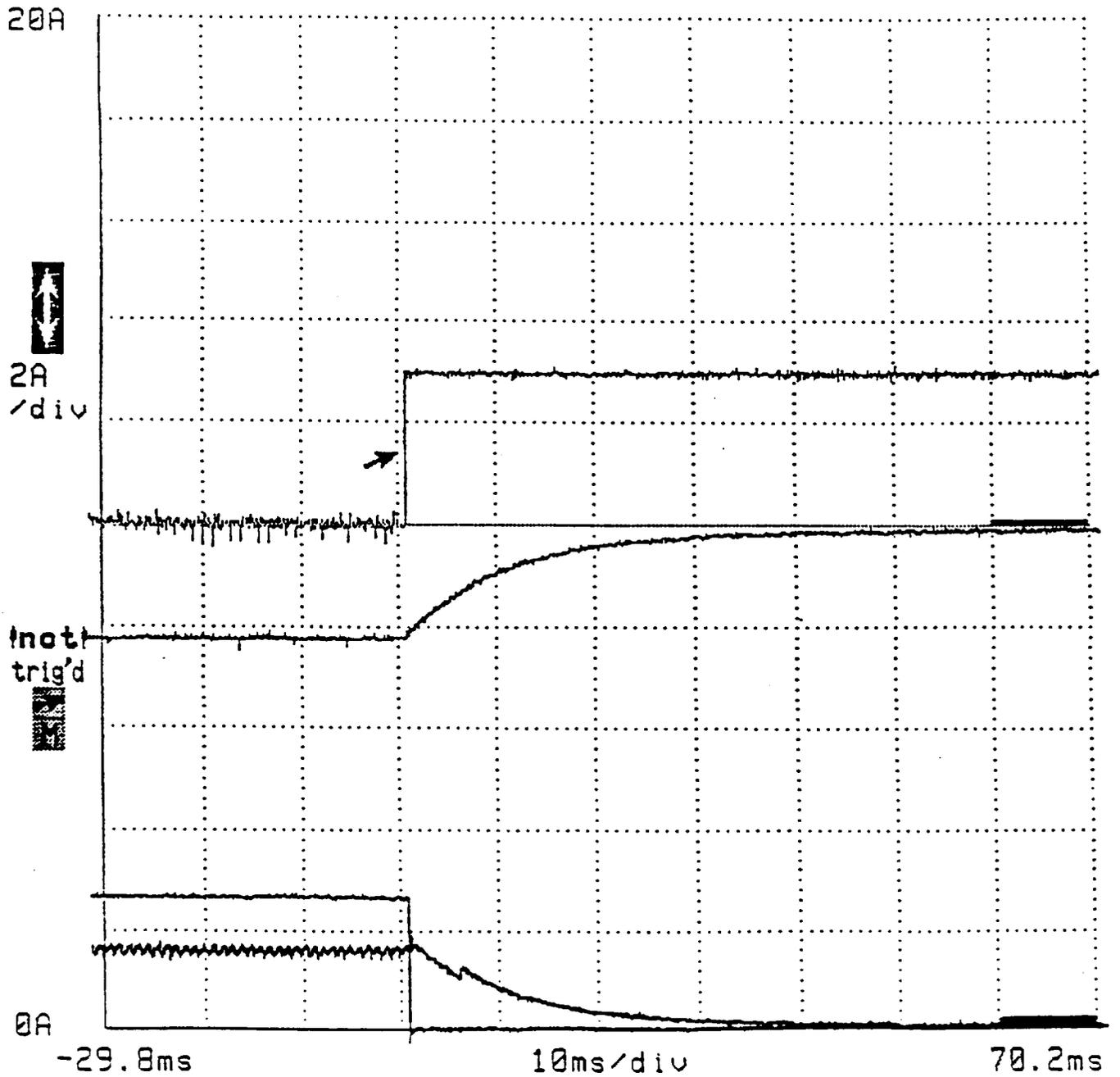


Fig. 2 Fault transient, LV-to-HV through 100 ohms.

Upper: Logic indicating converter shutdown
 LV output voltage at 200 V/div, baseline at center

Lower: HV inductor current at 2 A/div
 HV output voltage at 1 kV/div

Timebase: 10 ms/div

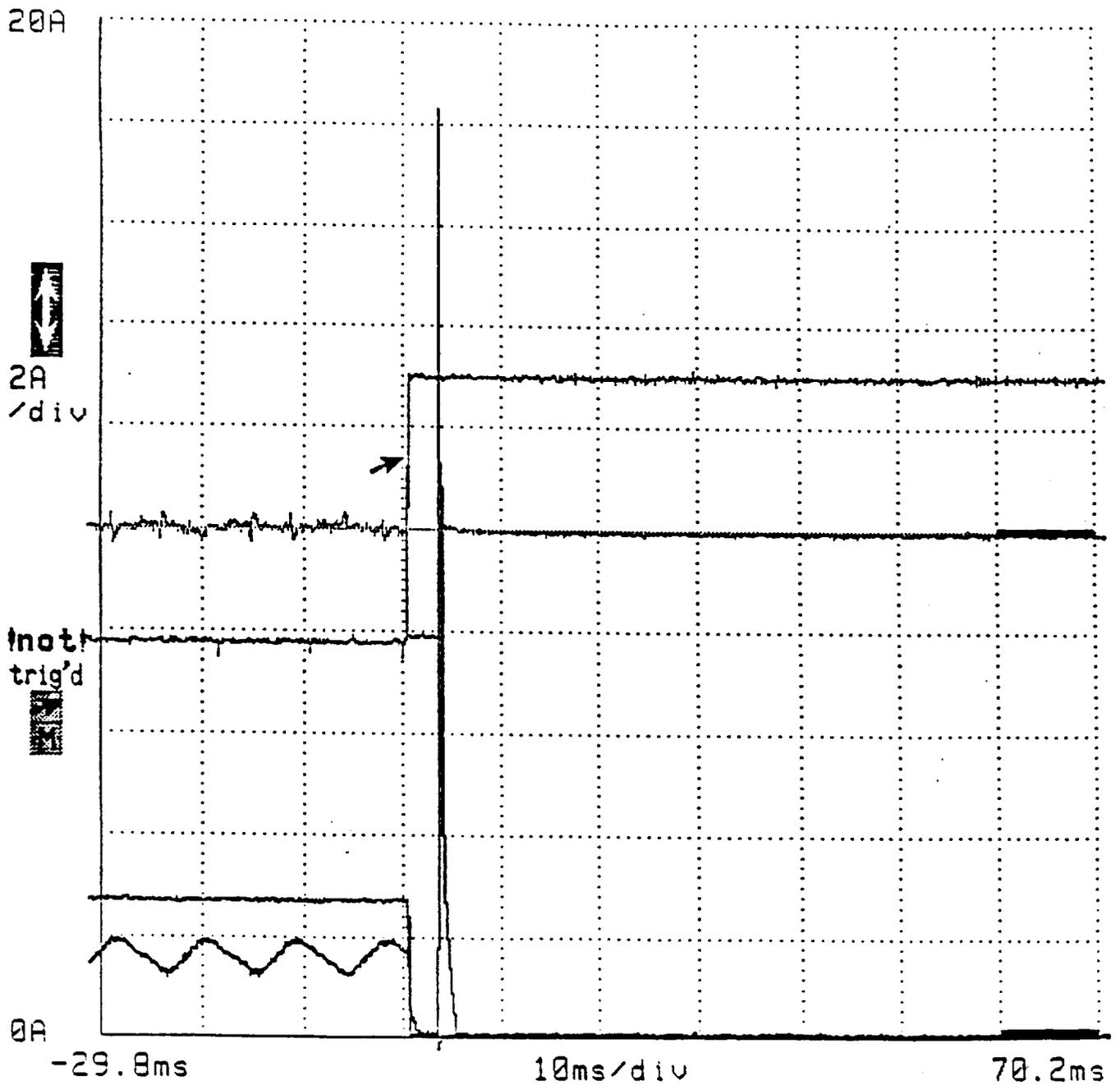


Fig. 3 Fault transient, LV-to-HV through dead short.

Upper: Logic indicating converter shutdown
 LV output voltage at 200 V/div, baseline at center

Lower: HV inductor current at 2 A/div
 HV output voltage at 1 kV/div

Timebase: 10 ms/div

Chapter 5

SUMMARY

A complete laboratory breadboard version of a ion engine power converter was built and tested. This prototype operated on a line voltage of 80-120 Vdc, and provided output ratings of 1100 V at 1.8 kW, and 250 V at 20 mA. The HV output voltage rating was revised from the original value of 1350 V at the beginning of the project. The LV output was designed to hold up during a 1-A surge current lasting up to 1 second. The prototype power converter included a internal housekeeping power supply which also operated from the line input. The power consumed in housekeeping is included in the overall energy budget presented for the ion engine converter. HV and LV output voltage setpoints are commanded through potentiometers.

The HV converter itself reached its highest power efficiency of slightly over 93% at low line and maximum output. This would dip below 90% at high line. The no-load (rated output voltages, zero load current) power consumption of the entire system was less than 13 W.

A careful loss breakdown shows that the converter losses are predominately MOSFET conduction losses and HV rectifier snubbing losses, with the rectifier snubbing losses becoming predominant at high line. This suggests that further improvements in power efficiency could best be obtained by either developing a rectifier that was adequately protected against voltage overshoot with less snubbing, or by developing a pre-regulator to reduce the range of line voltage on the converter.

The transient testing showed the converter to be fully protected against load faults, including a direct short-circuit from the HV output to the LV output terminals. Two current

sensors were used: one to directly detect any core ratcheting on the output transformer and re-initiate a soft start, and the other to directly detect a load fault and quickly shut down the converter for load protection. The finished converter has been extensively fault tested without failure.

The finished converter has been packaged suitable for use as a laboratory prototype for further testing. The finished converter is readily transportable.

Further work on this converter should probably concentrate on improving its power efficiency. This appears to be best done through development of a pre-regulator stage to reduce the peak voltage stress appearing in the HV rectifier. It is believed that any power loss introduced in the pre-regulator would be more than recovered in a redesigned output rectifier.

APPENDIX A

the following paper was presented at the

30th Intersociety Energy Conversion Engineering Conference

July 31 - August 4, 1995

Orlando, Florida

DESIGN ISSUES FOR HIGH VOLTAGE CONVERTERS
FOR ION ENGINES

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ABSTRACT

A design strategy is presented for a power converter for a high voltage ion engine for a spacecraft application. Various design issues such as appropriate topologies and control methods are considered. In this particular instance it was determined that a full bridge converter with phase shift gating and voltage mode control provided an efficient system with a minimum of EMI interference. This system can be implemented in a straightforward manner, and it is relatively easy to protect from faults at the output.

I. INTRODUCTION

The design constraints for space power converters differ from those of terrestrial converters in the following manner: (1) low mass is important because of the high cost of boosting it into space, but (2) high power efficiency is even more important because of the incremental mass in the heat removal system associated with a lower efficiency converter. High switching frequency is only useful to the extent that it allows weight reduction in the complete system comprising the switching converter and its heat removal system. Ion engine requirements then introduce additional complexities, primarily because of their exceptionally high voltages.

This study included a survey of various DC/DC converter topologies in order to select the most appropriate ones for a 2 kW ion engine power supply. This supply actually consists of two converters that provide the following power sources:

1. A 2 kW source with an output of 500-1350 V dc.
2. A 150-250 V dc source that delivers 20 mA steady state and a 1 A surge current.

In addition to selecting the topologies for these converters, their implementation often required a choice from several different technical options. A number of subtle problems also were encountered, and these frequently determined which

technology was used. The more important choices and problems are discussed in the next section, and it is hoped that some of this information will be useful in the design of power supplies for future ion thrusters.

II. TOPOLOGY AND CONTROL ISSUES

Several factors determined the choice of the converter for the 2 kW source:

1. DC isolation between input and output
2. Input and output voltage levels
3. Power level
4. Component limitations
5. Efficiency
6. Low mass
7. Reliability

The need for DC isolation obviously restricts the choice to a topology with a transformer. Actually, the high voltage transformation ratio (which has a maximum value of 1350/80) also would dictate this choice. The next basic decision is to select a circuit from the wide variety of forced switching and resonant topologies. The low switching loss of FETs virtually eliminates the need for relatively complex resonant circuits such as the series and parallel loaded types. VDS limitations of FETs then point to the full bridge topology.

Once the full bridge is selected, one must then decide between diagonal and phase-shift control. Diagonal is the simplest, but phase-shift readily allows the implementation of zero voltage switching (ZVS) for the FETs over the upper end of the load range [1-3], and it was selected for this reason. The schematic of the full bridge power circuit is shown in Fig. 2, while the drive signals for both diagonal and phase shift control are shown in Fig. 3. For a typical half cycle with phase shift control, Q1 and Q4 commence conducting together, but Q4 turns off first. As Q4 turns off, its drain current is diverted to C2 and C4 so that vDS increases at a slower rate, thus approximating ZVS. When Q1 turns off, C1 and C3 provide ZVS in a similar manner to C2 and C4. To avoid high turn-on losses, all of these capacitors must

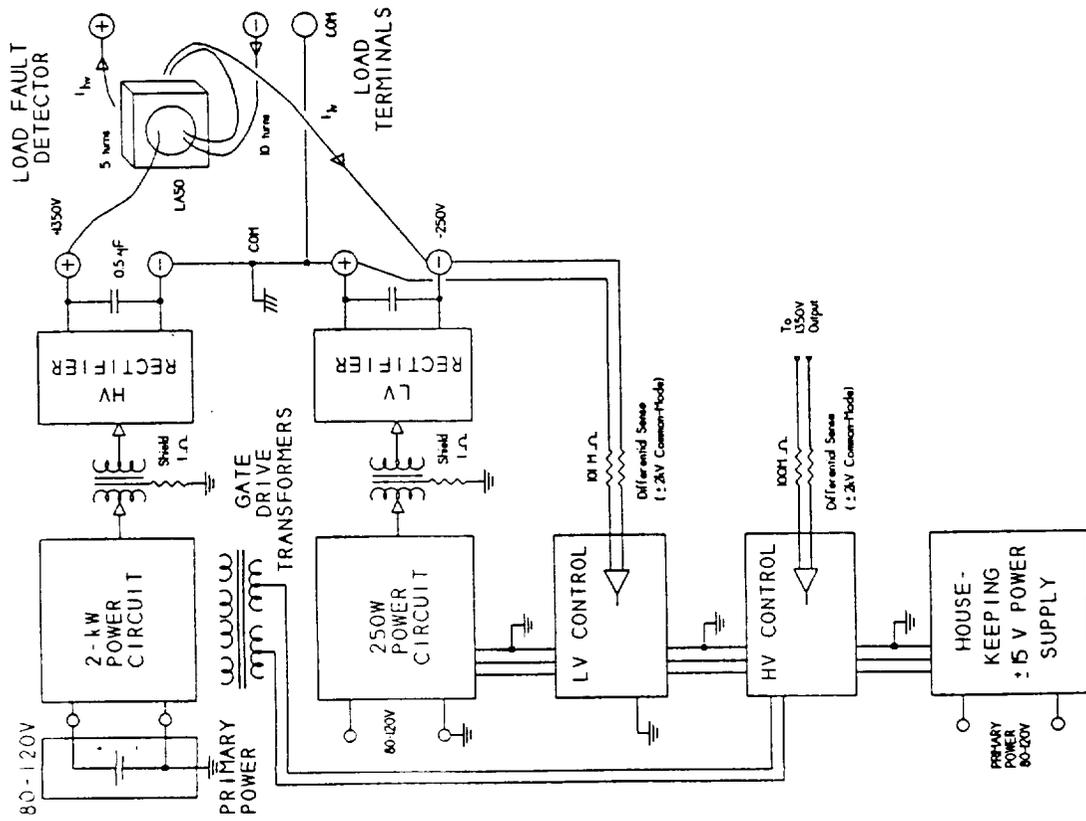


FIG. 1 SYSTEM BLOCK DIAGRAM - GROUNDING AND ISOLATION

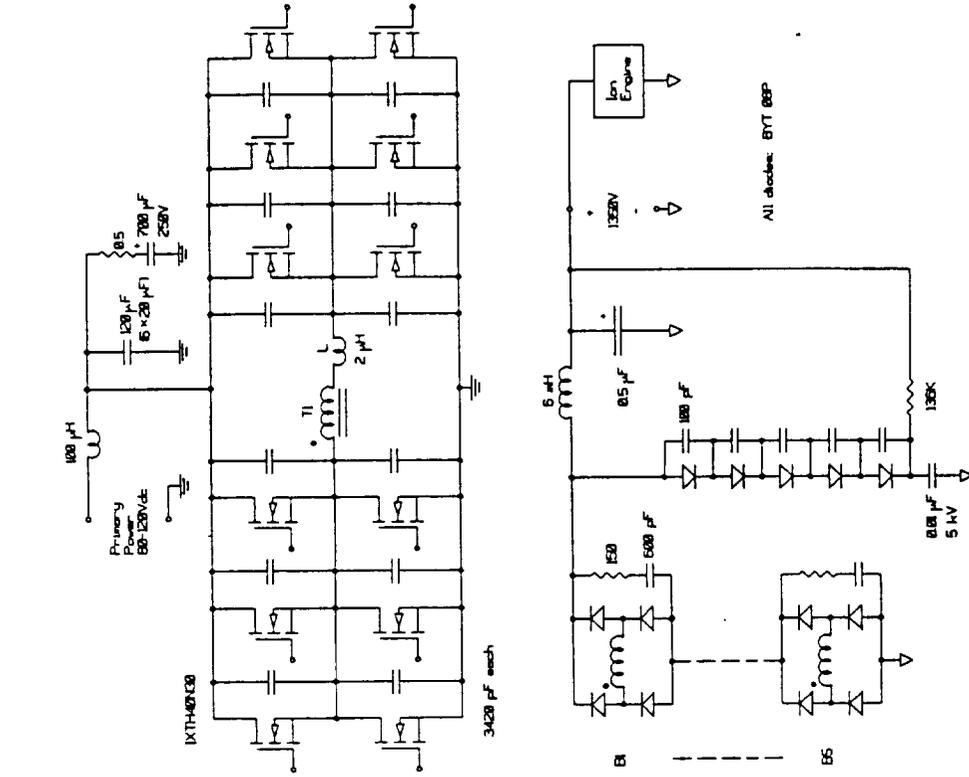


FIG. 2 2 kW POWER CIRCUIT

be properly charged before the start of the Q2-Q3 half cycle, i.e., C2 and C3 must be discharged and C1 and C4 must be charged to V_s . This is more difficult to achieve for C1 and C3 since their former charge must be "pumped" back into V_s by the energy stored in L1 and the leakage L of T1. Thus if C1-C4 are all the same size, Q1 and Q3 will experience higher turn-on losses than Q2 and Q4 when the load is reduced.

The next choice is between,

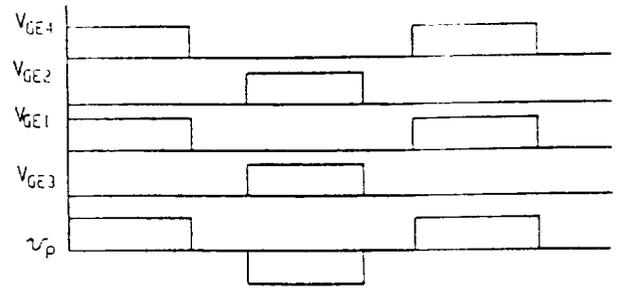
1. Current mode control (CMC) [4-6]
2. Average current mode control (ACMC) [7]
3. Voltage mode control (VMC) [6]

First, one should be aware that all bridge and push-pull circuits must guard against momentary flux imbalances that can lead to transformer saturation. If this happens, the transformer primary appears as a very low impedance, and if the circuit is unprotected the results are usually catastrophic.

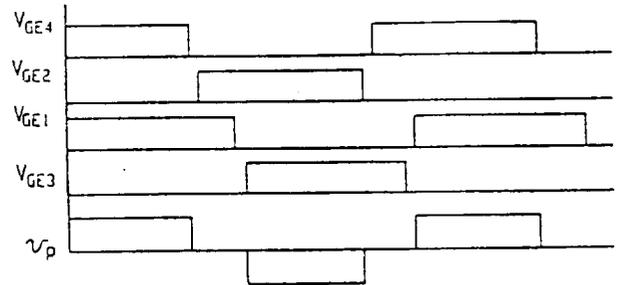
One possibility is to place a large capacitor in series with the primary, but at higher power levels this capacitor produces serious heating, mass and efficiency problems. CMC is also a popular solution to this problem, and it provides wide bandwidth which helps improve the transient response. However, CMC demands a sanitized replica of the load current waveform (e.g., minus turn-on transients and EMI) for the control circuit, and obtaining this can be tedious. CMC is certainly do-able, but the difficulty in obtaining the waveform replica at higher power levels motivates the search for a simpler approach.

ACMC was considered, but to provide flux balance this also requires an altered current feedback signal that responds to the instantaneous current as well as the average value. This approach was investigated, but it was eventually abandoned because of transients and EMI problems.

Because of the implementation complexities of CMC and ACMC, it was decided to investigate VMC for this application. VMC alone is always vulnerable to transformer saturation, but the circuit was altered to avoid this, and the resulting system appears to be less sensitive to transients and EMI than either CMC or ACMC. First of all, for steady state operation there are some factors that help to prevent transformer saturation. To explain this, it should be recognized that the conduction time periods and parasitic voltage drops the two halves of the circuit are always slightly imbalanced. This means that the transformer core will operate toward one end of its BH loop, and the magnetizing current will be higher for this half cycle than for the other. At the end of this half cycle, the magnetizing current will continue to increase as the end of the BH loop is approached, and the increasing iR drop will decrease the voltage applied to the winding. It is this increased iR drop that forces the flux to ultimately balance for the two half cycles, and the core will then operate on a steady state minor BH loop. This is perfectly acceptable as long as the increased magnetizing current on the one half cycle doesn't become excessive. As opposed to minority carrier devices such as BJTs, FETs are very helpful in limiting the magnetizing current because they are resistive and have positive temperature coefficients. They also minimize conduction time imbalances between the two half cycles because their switching times are very small, and thus any time imbalance is very small compared to a half period. If the saturation current on one half cycle is still too high, it can often be decreased to an acceptable level by increasing the gap in the transformer core. This increases the magnetizing current so the necessary iR increase can be achieved at a lower flux, which helps to avoid excessive saturation. In this particular application, acceptable steady state operation was achieved without increasing the transformer gap.



(a) Diagonal PWM



(b) Phase shift PWM

FIG. 3 PWM TIMING DIAGRAMS

Although features such as parasitic R and core gaps can provide satisfactory steady state operation, they cannot guarantee the avoidance of extreme saturation during transient conditions. Thus saturation may still randomly occur during situations such as start-up or output faults. To avoid FET failures during these conditions an active circuit must be used to protect the FETs. In this case a current sensor and controller was used to detect excessive primary currents, turn-off the circuit, and then use a soft re-start. In spite of this extra circuitry, the resulting VMC system was judged to be easier to implement than a CMC or an ACMC system. As noted earlier, stabilization of VMC requires a lower bandwidth than CMC or ACMC, and thus a slower transient response results. The transient response was still considered to be adequate for this application however, and this was not judged to a serious limitation.

The original controller for the 2 kW converter used the UC3875 control chip. Although simple to implement, this chip had very poor EMI immunity and was abandoned. A second controller was implemented with discrete ICs and used a control strategy very similar to that in the 3875. No serious EMI problems were encountered with this new controller.

III. IMPLEMENTATION

A block diagram of the complete system is shown in Fig. 1. The system provides the following outputs:

1. +500 TO 1350 V dc, 2 kW (HV Output)
2. -150 to -250 V dc, 250 W for 100 ms (LV Output)

Short circuit protection is provided for faults between either output and COM or between the two outputs. In the event of a fault, this protection circuitry is designed to de-energize the system, and it must be re-started manually. This requirement is in contrast to the usual practice of using a current limit mode that provides automatic recovery.

TABLE 1

STEADY-STATE-OPERATING PERFORMANCE OF THE ION ENGINE POWER CONVERTER

	Input Voltage/ Current	Input Power	Output Voltage/ Current	Output Power	Power Efficiency
Full Load Low Line	80V/ 25.6 A	2040W	1353V/ 1.38 A 248 V/O A	1867W	91.5%
Full Load High Line	120V/ 17.4A	2092W	1354V/ 1.38A 248 V/OA	1869W	89.3%
Partial Load Low Line	80V/ 11.7A	937 W	1352V/ 0.62 A 251 V/OA	838 W	89.4%
No Load High Line	120V/ 0.10A	12 W	1350V 250 V	---	---

The HV power circuit in Fig. 2. employs three paralleled 300 V FETs in each leg of a full wave bridge. A layered interconnect structure is used on the primary in order to minimize parasitic inductance.

The transformers used in most bridge and push-pull converters invariably have leakage inductances, L_l , that are larger than desired. Thus the usual design strategy should minimize L_l , and that was done in this case for the HV transformer. This was achieved by using a 3 turn foil winding on one leg of a UU core, wrapping this with a layer of insulation, and then winding the secondary in single layer sectors directly on top of the insulation. This achieved an $L_l = 0.5 \mu\text{H}$ when measured on the primary. Unfortunately this inductance was actually too low and resulted in an excessive current transient at turn-on. To reduce this transient to an acceptable level, it was necessary to add an external inductance of $2 \mu\text{H}$ in series with the primary.

If the transformer was re-designed, it would be advantageous to use a more compact arrangement, perhaps with more turns of multi-layer windings on a smaller core. This should reduce the weight and increase L_l to the desired value. The switching frequency of 60 kHz was selected primarily to provide a sufficiently low flux density in the transformer core. To accommodate the 1350 V dc output at this frequency, it was necessary to use 5 rectifier bridges connected in series as shown in Figure 2. Even with 600-V diodes, switching voltage transients required the use of substantial snubbers for these rectifiers. It was originally thought that this problem would be alleviated by use of the RHRU150100 diode because of its low t_{rr} and soft recovery characteristic. However, this diode is designed for currents well in excess of the 1.8 Adc maximum load current, and it has a large wafer with a high junction capacitance. This produced both current and voltage transients that were excessive and could not be reduced to satisfactory levels with reasonable snubbers. Thus it was necessary to resort to the MUR460 diode with its lower junction capacitance even though it does not have soft recover.

The LV converter has a maximum steady state load of only 5 W and this could be derived from a small converter. However, it also has to supply a 1 A surge for 100 ms with less than a 50% voltage droop. If a very small converter was used, this surge specification would require the use of an extremely large output capacitor. Instead of supplying this pulse from a capacitor, it was determined that considerable weight and volume could be saved by designing the converter itself to supply a 1 A surge for 100 ms. Although this necessitates much larger semi-conductors in the converter, the complete weight and volume are much less than the large capacitor version. The converter now has a 100 ms rating of 250 W but this is still within the range where simpler topologies are effective. Therefore a relatively simple forward converter was selected for this circuit.

IV. EXPERIMENTAL RESULTS

The experimental hardware was initially constructed using average inductor-current control in an attempt to ensure transformer flux balancing. By the use of a dc-coupled current sensor (LEM LA-50) placed in the transformer primary, and sufficient current-loop bandwidth to have switching-frequency ripple appear at the input to the pulse-width modulator (PWM), it was possible to achieve flux balance over a range of operating conditions. Unfortunately, the result obtained was impaired due to the presence of underdamped ringing in the transformer primary current. This ringing, caused by the resonance of the high-voltage rectifier diode's junction capacitance with the transformer leakage inductance, also appeared at the PWM input, thus interfering with a stable balance of the two switching half-cycles. Because the amplitude of the ringing component of primary current is essentially proportional to the line voltage, while the expected quasi-square primary current is determined by the load current, it was found that satisfactory flux balance would not occur at light load and high line. It was also noted that a latch-up mode involving a sustained sub-harmonic oscillation was possible as an outgrowth of the large ringing components appearing at the PWM.

Sufficient damping of the ringing currents to solve the stability problem was not possible without excessive loss penalties. Reduction of the current-loop bandwidth would stabilize the system, but this eliminated its flux-balancing effects. Low-bandwidth current feedback offered no other advantage and was therefore abandoned. Future availability of improved high-voltage rectifiers may allow reconsideration of current feedback.

The steady-state operating performance is summarized in Table 1.

Key waveforms for the trailing leg MOSFETs in operation at 1300 V/1.89 kW output are shown in Fig. 4. The drain current is inaccessible, but close examination of the gate and drain voltage waveforms shows that ZVS is being obtained at turn-off and turn-on. The transformer primary current waveform shows significant ringing current. Below one-half rated output current, the ringing was found to interfere with ZVS. The switching frequency is 55 kHz, giving an output ripple frequency of 110 kHz.

A multiple-level protection philosophy is used. The MOSFET on-resistances were found adequate for transformer flux balancing under all steady-state conditions. However, a dc-coupled primary current sensor is used to reset the converter if the primary current exceeds a preset limit. Reset is followed by a soft-start ramp-up of the output voltage set point. The load current is also monitored by a dc-coupled sensor which causes a latched shutdown of the converter in the case of a load fault. This sensor detects the sum of the output currents at the high

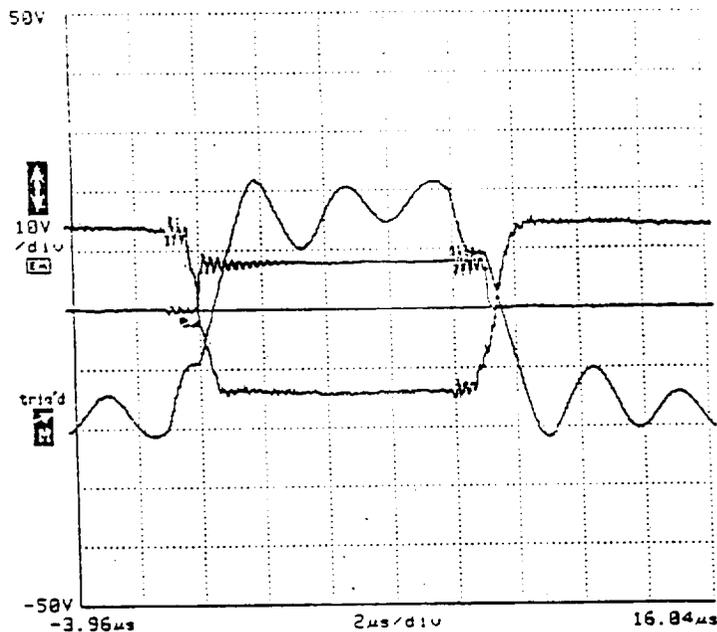


FIG. 4 COMMUTATION OF TRAILING LEG MOSFET.
INPUT VOLTAGE 80 V;
OUTPUT VOLTAGE 1300 V AT 1.89 kW.

GATE-SOURCE: 10V/DIV
DRAIN-SOURCE VOLTAGE: 100 V/DIV
TRANSFORMER PRIMARY CURRENT: 20 A/DIV

voltage and low voltage terminals and trips if the following condition is satisfied:

$$5 I_{HV} + 10 I_{LV} > 20 \text{ A.} \quad (1)$$

The predominant fault with the ion engine is considered to be arcing from the high voltage to the low voltage terminal. The arrangement of (1) gives excellent protection against this fault mode with a single sensor (the fault current appears in both I_{HV} and I_{LV}), while also giving protection against a fault to ground of either the low-voltage or the high voltage power supply. The sensor is implemented using two windings on a single Hall-effect-based device. The low-voltage converter is further protected by internal pulse-by-pulse current limiting roughly equivalent to a 1-A output surge. The low-voltage converter is able to survive this current surge electrically, and thermally for some 30-60 seconds, more than enough to handle normal start-up currents in the ion engine.

The transient behavior of the ion engine power supply is shown in Fig. 5, which shows the effect of a 0- Ω short-circuit applied between the +1350 V and the -250 V output terminals. The waveforms are (from top to bottom): a logic waveform indicating detection of the fault and shutdown, the low-voltage output (200 V/div), the high voltage output (1 kV/div), and the current in the high-voltage filter inductor (2 A/div). The line voltage is 120 V. The detection of the fault and the collapse of the high-side output voltage are almost simultaneous due the smaller filter capacitor on the +1350-V output.

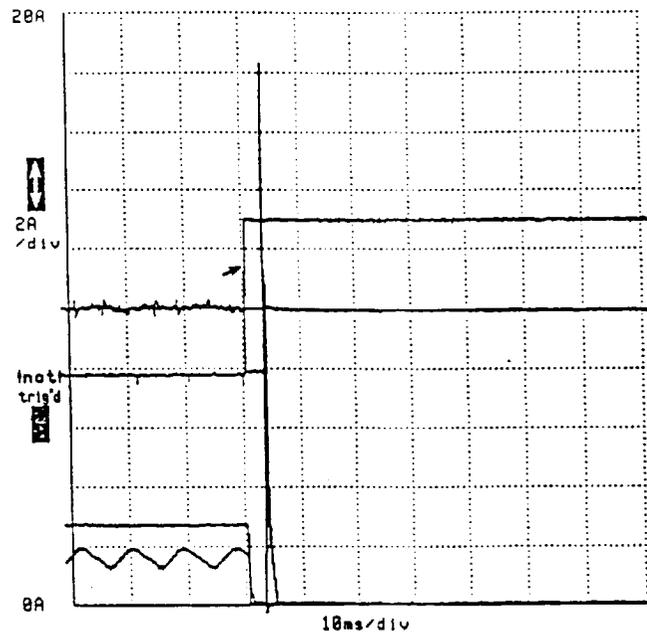


FIG. 5 LOAD FAULT TRANSIENT: 0 Ω APPLIED FROM HV
TO LV OUTPUT TERMINAL LINE
VOLTAGE 120 V.

UPPER GROUP:
LOGIC SIGNAL INDICATING DETECTION OF
FAULT AND CONVERTER SHUTDOWN
LV OUTPUT VOLTAGE: 200 V/DIV

LOWER GROUP:
HV OUTPUT VOLTAGE: 1 kV/dDIV
HV FILTER INDUCTOR CURRENT: 2 A/DIV

However, the -250 V holds up for about 4 ms, after which it abruptly collapses simultaneously with a large impulse of current in the high-side inductor. It is postulated that the high-side inductor supports the low-side output voltage until it saturates, and subsequently permits rapid discharge of the energy stored in the 120 μ F low-side filter capacitor. This behavior argues against using an excessively large storage capacitor to meet the low-side transient output current requirements. The 15 A discharge observed in this test is well within the capability of the high-voltage diodes.

An anomalous ripple may be observed in the high-voltage inductor current of Fig. 5. Although the ripple amplitude is correct, the ripple frequency appears to be only 110 Hz. This illustrates a hazard of using a digital sampling oscilloscope. The actual ripple frequency of 110 kHz has been aliased in this figure due to the limited sampling rate possible at the sweep speed in use.

V. SUMMARY

An ion engine power supply system has been built and tested with good results. It was found that transformer flux balancing problems could be solved using simple voltage loop control, with the MOSFET on-resistances providing the needed balancing force under normal conditions. A peak current detector in the transformer primary provides back-up protection against transient saturation by triggering a soft restart. This

back-up circuit was never observed to operate during ordinary conditions, such as start-up, load dump and load connection. The ion engine power supply was readily made short-circuit safe, as evidenced by considerable laboratory testing.

Soft switching of the MOSFET's was obtained for output currents exceeding 50 percent of full load, although ringing in the transformer primary current made soft-switching problematic at light load. This ringing was caused by the interaction of the transformer leakage inductance, added to obtain soft switching, and the high-voltage diode's junction capacitance. This ringing also made current-mode control impractical to implement. Diodes having lowered junction capacitance would allow rethinking of these conclusions. It was also found necessary to add considerable dissipative snubbing to control voltage overshoots at the output rectifier diodes. Therefore, improvement in the system efficiency would also result from diodes having lowered capacitances.

It is believed that future development efforts should focus on a preregulator as the way to obtain wide line voltage capability while maintaining good power efficiency. The need for an increased transformer turns ratio to obtain low line operation causes considerable increase in the peak voltage on the rectifier diodes. A non-isolated boost regulator in the 80-120 V input line can achieve high efficiencies using presently available components. It is postulated that the additional losses of an added boost converter would be more than offset by lowered losses in the output rectifiers.

ACKNOWLEDGEMENT

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