High-Performance Spaceflight Computing (HPSC) Program Overview

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<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>AFRL</td>
<td>Air Force Research Laboratory</td>
<td>GB/s</td>
<td>Gigabytes Per Second</td>
</tr>
<tr>
<td>AMBA</td>
<td>ARM Advanced Microcontroller Bus Architecture</td>
<td>GNC</td>
<td>Guidance Navigation and Control</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
<td>GOPS</td>
<td>Giga Operations Per Second</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
<td>GSFC</td>
<td>Goddard Space Flight Center</td>
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<tr>
<td>CFS</td>
<td>Core Flight Software</td>
<td>HEOMD</td>
<td>Human Exploration and Operations Directorate</td>
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<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
<td>HPSC</td>
<td>High Performance Spaceflight Computing</td>
</tr>
<tr>
<td>C&amp;DH</td>
<td>Command and Data Handling</td>
<td>JPL</td>
<td>Jet Propulsion Laboratory</td>
</tr>
<tr>
<td>DDR</td>
<td>Double Data Rate</td>
<td>KHz</td>
<td>Kilohertz</td>
</tr>
<tr>
<td>DMR</td>
<td>Dual Modular Redundancy</td>
<td>Kpps</td>
<td>Kilo Packets Per Second</td>
</tr>
<tr>
<td>DRAM</td>
<td>Dynamic Random Access memory</td>
<td>Mbps</td>
<td>Megabits Per Second</td>
</tr>
<tr>
<td>EEPROM</td>
<td>Electrically Erasable Programmable Read-Only Memory</td>
<td>MCM</td>
<td>Multi Chip Module</td>
</tr>
<tr>
<td>FCR</td>
<td>Fault Containment Region</td>
<td>MRAM</td>
<td>Magnetoresistive Random Access Memory</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
<td>NASA</td>
<td>National Aeronautics and Space Administration</td>
</tr>
<tr>
<td>FSW</td>
<td>Flight Software</td>
<td>NVRAM</td>
<td>Nonvolatile Random Access memory</td>
</tr>
<tr>
<td>Gb/s</td>
<td>Gigabits Per Second</td>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>HEOMD</td>
<td>Human Exploration and Operations Directorate</td>
<td>SCP</td>
<td>Self Checking Pair</td>
</tr>
<tr>
<td>HPSC</td>
<td>High Performance Spaceflight Computing</td>
<td>SRAM</td>
<td>Static Random Access memory</td>
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<td>JPL</td>
<td>Jet Propulsion Laboratory</td>
<td>SRIIO</td>
<td>Serial RapidIO</td>
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<tr>
<td>KHz</td>
<td>Kilohertz</td>
<td>SSR</td>
<td>Solid State Recorder</td>
</tr>
<tr>
<td>Kpps</td>
<td>Kilo Packets Per Second</td>
<td>STMD</td>
<td>Space Technology Mission Directorate</td>
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<tr>
<td>Mbps</td>
<td>Megabits Per Second</td>
<td>TTE</td>
<td>Time Triggered Ethernet</td>
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<tr>
<td>MCM</td>
<td>Multi Chip Module</td>
<td>TTGbe</td>
<td>Time Triggered Gigabit Ethernet</td>
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<tr>
<td>MRAM</td>
<td>Magnetoresistive Random Access Memory</td>
<td>TMR</td>
<td>Triple Modular Redundancy</td>
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<tr>
<td>NASA</td>
<td>National Aeronautics and Space Administration</td>
<td>TRCH</td>
<td>Timing Reset Configuration and Health</td>
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<tr>
<td>NVRAM</td>
<td>Nonvolatile Random Access memory</td>
<td>XAUI</td>
<td>10 Gigabit Media Independent Interface</td>
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<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
<td>VMC</td>
<td>Vehicle Management Computer</td>
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<td>Nonvolatile Random Access memory</td>
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<td>PCB</td>
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Outline

• HPSC Overview
• HPSC Contract
• Chiplet Architecture
• HPSC Middleware
• NASA HPSC Use Cases
High Performance Spaceflight Computing (HPSC) Overview

• The goal of the HPSC program is to dramatically advance the state of the art for spaceflight computing

• HPSC will provide a nearly two orders-of-magnitude improvement above the current state of the art for spaceflight processors, while also providing an unprecedented flexibility to tailor performance, power consumption, and fault tolerance to meet widely varying mission needs

• These advancements will provide game changing improvements in computing performance, power efficiency, and flexibility, which will significantly improve the onboard processing capabilities of future NASA and Air Force space missions

• HPSC is funded by NASA's Space Technology Mission Directorate (STMD), Science Mission Directorate (SMD), and the United States Air Force

• The HPSC project is managed by Jet Propulsion Laboratory, and the HPSC contract is managed by NASA Goddard Space Flight Center (GSFC)
HPSC Background

- HPSC began with a NASA internal study, which identified several use cases for high performance spaceflight computing

<table>
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<tr>
<th>Human Spaceflight (HEOMD) Use Cases</th>
<th>Science Mission (SMD) Use Cases</th>
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<tr>
<td>Cloud Services</td>
<td>Extreme Terrain Landing</td>
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<tr>
<td>Advanced Vehicle Health Management</td>
<td>Proximity Operations / Formation Flying</td>
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<tr>
<td>Crew Knowledge Augmentation Systems</td>
<td>Fast Traverse</td>
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<tr>
<td>Improved Displays and Controls</td>
<td>New Surface Mobility Methods</td>
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<tr>
<td>Augmented Reality for Recognition and Cataloging</td>
<td>Imaging Spectrometers</td>
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<tr>
<td>Tele-Presence</td>
<td>Radar</td>
</tr>
<tr>
<td>Autonomous &amp; Tele-Robotic Construction</td>
<td>Low Latency Products for Disaster Response</td>
</tr>
<tr>
<td>Automated Guidance, Navigation, and Control (GNC)</td>
<td>Space Weather</td>
</tr>
<tr>
<td>Human Movement Assist</td>
<td>Science Event Detection and Response</td>
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<td></td>
<td>Immersive Environments for Science Ops / Outreach</td>
</tr>
</tbody>
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- Following this study, a AFRL/NASA Next Generation Space Processor (NGSP) analysis program engaged industry to define and benchmark future multi-core processor architectures

- Based on the results of this program, the Government generated the conceptual reference architecture and detailed requirements for the HSPC “Chiplet”
HPSC Background

- Reference design features power-efficient **ARM 64-bit processor cores (8)** and on-chip interconnects scalable and extensible in MCM (Multi-Chip Module) or on PCB (Printed Circuit Board) via XAUI and SRIO (Serial RapidIO) 3.1 high-speed links

  - Multi-Chiplet configurations (tiled or cascaded) provide increased processing throughput and/or increased fault tolerance (e.g. each Chiplet as separate fault containment regions, NMR)
  - Chiplets may be connected to other XAUI/SRIO devices
    - e.g. FPGAs, GPUs, or ASIC co-processors

- Supports multiple hardware-based and software-based fault tolerance techniques
Following a competitive procurement, the HPSC cost-plus fixed-fee contract was awarded to Boeing.

Under the base contract, Boeing will provide:
- Prototype radiation hardened multi-core computing processors (Chiplets), both as bare die and as packaged parts
- Prototype system software which will operate on the Chiplets
- Evaluation boards to allow Chiplet test and characterization
- Chiplet emulators to enable early software development

Five contract options have been executed to enhance the capability of the Chiplet:
- On-chip Level 3 cache memory
- Dual real-time processors
- Dual Time Triggered Ethernet (TTE) interfaces
- Dual SpaceWire interfaces
- Package amenable to spaceflight qualification

Contract deliverables are due April 2021.
Chiplet Architecture

- With the contract options awarded and the preliminary design completed, the Chiplet architecture has evolved from the original reference architecture.

HPSC Chiplet Architecture
• AFRL is funding JPL and NASA GSFC to develop HPSC Middleware

• Middleware will provide a software layer that provides services to the higher-level application software to achieve:
  - Configuration management
  - Resource allocation
  - Power/performance management
  - Fault tolerance capabilities of the HPSC chiplet

• Serving as a bridge between the upper application layer and lower operating system or hypervisor, the middleware will significantly reduce the complexity of developing applications for the HPSC chiplet

INTEGRATED STACK CONCEPT

Mission Applications

FSW Product Lines – Core S/C Bus Functions
GSFC and JPL Core Flight Software (CFS)

HPSC Middleware – Resource Management
Mission-Friendly Interface for Managing/Allocating Cores for Performance vs. Power vs. Fault Tolerance

Traditional System Software – RTOS or Hypervisor, FSW Development Environment

Hardware – Multi-core Processor Chips, Evaluation Boards
To be presented at Space Computing & Connected Enterprise Resiliency Conference (SCCERC), Bedford, MA, June 4-8, 2018.

**HPSC Use Cases**

### Rover

**Compute Needs**
- Vision Processing
- Motion/Motor Control
- GNC/C&DH
- Planning
- Science Instruments
- Communication
- Power Management
- Thermal Management
- Fault detection/recovery

**System Metrics**
- 2-4 GOPs for mobility (10x RAD750)
- >1Gb/s science instruments
- 5-10GOPs science data processing
- >10KHz control loops
- 5-10GOPS, 1GB/s memory BW for model based reasoning for planning

### Lander

**Compute Needs**
- Hard Real time compute
- High rate sensors w/zero data loss
- High level of fault protection/fail over

**System Metrics**
- >10 GOPs compute
- 10Gb/s+ sensor rates
- Microsecond I/O latency
- Control packet rates >1Kpps
- Time tagging to microsecond accuracy
**High Bandwidth Instrument**

**Compute Needs**
- Soft real time
- Non-mission critical
- High rate sensors
- Large calibration sets in NV memory

**System Metrics**
- 10-20 GOPs compute
- >10GB/s memory bandwidth
- >20Gbps sensor IO data rates

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**Smallsat**

**Compute Needs**
- Hard and Soft real time
- GNC/C&DH
- Autonomy and constellation (cross link comm)
- Sensor data processing
- Autonomous science

**System Metrics**
- 2-5Gbps sensor IO
- 1-10GOPs
- 1GB/s memory bandwidth
- 250Mbps cross link bandwidth
Similar to Orion two fault tolerant architecture

- A single HPSC exceeds the performance metrics of a Orion Vehicle Management Computer (VMC)
- A VMC contains three Self-Checking Pairs (SCP)
Conclusion

• Future space mission scenarios call out for significantly improved spaceflight computing capability

• Improved spaceflight computing means enhanced computational performance, energy efficiency, and fault tolerance

• With the ongoing HPSC development, we are well underway to meeting future spaceflight computing needs

• The NASA-developed Middleware will allow the efficient infusion of the HPSC chiplet into those missions

• As illustrated by the NASA use cases, our future missions demand the capabilities of HPSC

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