High-Performance Spaceflight Computing (HPSC) Project Overview

Wesley Powell
Assistant Chief for Technology
NASA Goddard Space Flight Center
Electrical Engineering Division (Code 560)

wesley.a.powell@nasa.gov
301-286-6069

To be presented at Radiation Hardened Electronics Technology (RHET) Conference, Phoenix, AZ, November 5-8, 2018.
<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>AMBA</td>
<td>ARM Advanced Microcontroller Bus Architecture</td>
<td>DRAM</td>
<td>Dynamic Random Access memory</td>
<td>GPU</td>
<td>Graphics Processing Unit</td>
<td></td>
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<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
<td>DTRA</td>
<td>Defense Threat Reduction Agency</td>
<td>GSFC</td>
<td>Goddard Space Flight Center</td>
<td></td>
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<tr>
<td>BSP</td>
<td>Board Support Package</td>
<td>ECC</td>
<td>Error Correction Coding</td>
<td>HEOMD</td>
<td>Human Exploration and Operations Directorate</td>
<td></td>
<td></td>
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<tr>
<td>BW</td>
<td>Bandwidth</td>
<td>EEPROM</td>
<td>Electrically Erasable Programmable Read-Only Memory</td>
<td>HPPS</td>
<td>High Performance Processing Subsystem</td>
<td></td>
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<tr>
<td>CCN</td>
<td>Cache Coherent Network</td>
<td>FCR</td>
<td>Fault Containment Region</td>
<td>HPSC</td>
<td>High Performance Spaceflight Computing</td>
<td></td>
<td></td>
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<tr>
<td>CFS</td>
<td>Core Flight Software</td>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
<td>I2C</td>
<td>Inter-Integrated Circuit</td>
<td></td>
<td></td>
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<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
<td>FPU</td>
<td>Floating Point Unit</td>
<td>IDE</td>
<td>Integrated Development Environment</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C&amp;DH</td>
<td>Command and Data Handling</td>
<td>FSW</td>
<td>Flight Software</td>
<td>ISA</td>
<td>Instruction Set Architecture</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CDR</td>
<td>Critical Design Review</td>
<td>Gbd</td>
<td>Gigabaud</td>
<td>ISI</td>
<td>Information Sciences Institute</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DARPA</td>
<td>Defense Advanced Research Projects Agency</td>
<td>Gb/s</td>
<td>Gigabits Per Second</td>
<td>JPL</td>
<td>Jet Propulsion Laboratory</td>
<td></td>
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</tr>
<tr>
<td>DDR</td>
<td>Double Data Rate</td>
<td>GB/s</td>
<td>Gigabytes Per Second</td>
<td>JTAG</td>
<td>Joint Test Action Group</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DECTED</td>
<td>Double Error Correct Triple Error Detect</td>
<td>GHz</td>
<td>Gigahertz</td>
<td>KHz</td>
<td>Kilohertz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMEA</td>
<td>Defense Microelectronics Activity</td>
<td>GNC</td>
<td>Guidance Navigation and Control</td>
<td>Kpps</td>
<td>Kilo Packets Per Second</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMIPS</td>
<td>Dhrystone Million Instructions per Second</td>
<td>GOPS</td>
<td>Giga Operations Per Second</td>
<td>LET</td>
<td>Linear Energy Transfer</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
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</thead>
<tbody>
<tr>
<td>Mbps</td>
<td>Megabits Per Second</td>
</tr>
<tr>
<td>MeV</td>
<td>Million Electron Volt</td>
</tr>
<tr>
<td>MHz</td>
<td>Megahertz</td>
</tr>
<tr>
<td>MRAM</td>
<td>Magnetoresistive Random Access Memory</td>
</tr>
<tr>
<td>MT/s</td>
<td>Million Transfers per Second</td>
</tr>
<tr>
<td>mW</td>
<td>Milli Watt</td>
</tr>
<tr>
<td>NASA</td>
<td>National Aeronautics and Space Administration</td>
</tr>
<tr>
<td>NGSP</td>
<td>Next Generation Space Processor</td>
</tr>
<tr>
<td>nm</td>
<td>Nanometer</td>
</tr>
<tr>
<td>NVRAM</td>
<td>Nonvolatile Random Access memory</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PCIe</td>
<td>Peripheral Component Interconnect Express</td>
</tr>
<tr>
<td>PDR</td>
<td>Preliminary Design Review</td>
</tr>
</tbody>
</table>

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Outline

- HPSC Overview
- HPSC Contract
- Key Requirements
- Chiplet Architecture
- HPSC System Software and Middleware
- NASA HPSC Use Cases
- HPSC Ecosystem
High Performance Spaceflight Computing (HPSC) Overview

• The goal of the HPSC program is to dramatically advance the state of the art for spaceflight computing

• HPSC will provide a nearly two orders-of-magnitude improvement above the current state of the art for spaceflight processors, while also providing an unprecedented flexibility to tailor performance, power consumption, and fault tolerance to meet widely varying mission needs

• These advancements will provide game changing improvements in computing performance, power efficiency, and flexibility, which will significantly improve the onboard processing capabilities of future NASA and Air Force space missions

• HPSC is funded by NASA’s Space Technology Mission Directorate (STMD), Science Mission Directorate (SMD), and the United States Air Force

• The HPSC project is managed by Jet Propulsion Laboratory, and the HPSC contract is managed by NASA Goddard Space Flight Center (GSFC)
Initially provided in the Request for Proposal, a reference design features power-efficient ARM 64-bit processor cores (8) and on-chip interconnects scalable and extensible in MCM (Multi-Chip Module) or on PCB (Printed Circuit Board) via XAUI and SRIO (Serial RapidIO) 3.1 high-speed links

- Multi-Chiplet configurations (tiled or cascaded) provide increased processing throughput and/or increased fault tolerance (e.g. each Chiplet as separate fault containment regions, NMR)
- Chiplets may be connected to other XAUI/SRIO devices
  - e.g. FPGAs, GPUs, or ASIC co-processors

- Supports multiple hardware-based and software-based fault tolerance techniques
HPSC Contract

• Following a competitive procurement, the HPSC cost-plus fixed-fee contract was awarded to Boeing

• Under the base contract, Boeing will provide:
  ▪ Prototype radiation hardened multi-core computing processors (Chiplets), both as bare die and as packaged parts
  ▪ Prototype system software which will operate on the Chiplets
  ▪ Evaluation boards to allow Chiplet test and characterization
  ▪ Chiplet emulators to enable early software development

• Five contract options have been executed to enhance the capability of the Chiplet
  ▪ On-chip Level 3 cache memory
  ▪ Dual real-time processors
  ▪ Dual Time Triggered Ethernet (TTE) interfaces
  ▪ Dual SpaceWire interfaces
  ▪ Package amenable to spaceflight qualification

• Contract deliverables are due April 2021
Chiplet Architecture

- With the contract options awarded and the preliminary design completed, the Chiplet architecture has evolved from the original reference architecture.
HPSC Chiplet Program Overview

Program Structure & Schedule

• **Tasks (WBS Level 1)**

  1.0 Management
  2.0 System Engineering
  3.0 Chiplet Development
  4.0 System Software Development
  5.0 Evaluation Board Development
  6.0 Test and Characterization

• **Phases**

<table>
<thead>
<tr>
<th>Phase</th>
<th>Duration</th>
<th>Period of Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Preliminary Design</td>
<td>14 months</td>
<td>March 2017 through May 2018</td>
</tr>
<tr>
<td>2. Detailed Design</td>
<td>17 months</td>
<td>June 2018 through October 2019</td>
</tr>
<tr>
<td>3. Fabrication</td>
<td>9 months</td>
<td>November 2019 through July 2020</td>
</tr>
<tr>
<td>4. Test &amp; Characterization</td>
<td>9 months</td>
<td>August 2020 through April 2021</td>
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• **Schedule**

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## Key Requirements Summary

| **Processor Cores** | High Performance Processing Subsystem (HPPS): 8 ARM Cortex-A53 cores with floating point & Single Instruction Multiple Data (SIMD) engine. Performance & power on next slide
| | Real Time Processing Subsystem (RTPS) with single A53 and dual Cortex-R52 cores |
| **Memory Interfaces** | 3 DDR3/4: 2 for A53 clusters, 1 for RTPS
| | 4 SRAM/NV RAM
| | Enhanced error correction (ECC) to operate through bit upsets and whole memory device failures |
| **IO Interfaces** | 6 SRIO 3.1, 2 PCIe Gen2 serial IO
| | Ethernet, SpaceWire, Time Triggered Ethernet (TTE), SPI, UART, I²C, GPIO |
| **Power scaling** | Able to dynamically power down/up cores, subsystems, & interfaces via software control |
| **Fault tolerance** | Able to autonomously detect errors & log errors, prevent propagation past established boundaries, and notify software |
| **Trust & Assured Integrity** | DMEA-accredited Trusted supply chain
| | Free of malicious insertions / alterations |
| **Temperature** | -55C to 125C |
Performance @ Power Requirements

HPSC Chiplet Performance at Power

- **Scenario 1**: 9-15 GOPS* in 7-10 Watts with 50% IO Utilization, 50% Memory Utilization
- **Scenario 2**: 0.3 - 1 GOPS* in 0.5-1.0 Watts with 10% IO Utilization, 10% Memory Utilization
- **Scenario 3**: Sleep Mode < 100 mW

* GOPS not including SIMD engine performance

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# Key Requirements Summary

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Specification</th>
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<tbody>
<tr>
<td>Total Ionizing Dose (TID)</td>
<td>Strategic radiation hardness for Air Force applications</td>
</tr>
<tr>
<td>Prompt Dose Immunity</td>
<td></td>
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<tr>
<td>Dose Rate Survivability</td>
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<tr>
<td>Latchup Immunity</td>
<td>LET ≥ 90 MeV-cm²/mg</td>
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<tr>
<td>Single-Event Upset (SEU) (Adams 90% WC GEO)</td>
<td>HPPS (A53 Array): ≤ 1E-3 errors/device-day</td>
</tr>
<tr>
<td>Single-Event Upset (SEU) (WC Solar Flare)</td>
<td>RTPS: ≤ 1E-4 errors/device-day</td>
</tr>
<tr>
<td>Reliability</td>
<td>TRCH: ≤ 1E-5 errors/device-day</td>
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<tr>
<td>Reliability</td>
<td></td>
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<tr>
<td>≥ 100,000 power-on hours</td>
<td></td>
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<tr>
<td>Software</td>
<td></td>
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<tr>
<td>More core operating systems (Linux &amp; RTOS)</td>
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<tr>
<td>Development tools (compilers, debuggers, etc)</td>
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<tr>
<td>Board Support Packages (BSPs)</td>
<td></td>
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<tr>
<td>APIs for fault tolerance, power management</td>
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<tr>
<td>Emulators</td>
<td></td>
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<tr>
<td>Software-based quick emulator</td>
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<tr>
<td>FPGA-based cycle-accurate emulator</td>
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• **Develop Chiplet using Boeing’s RHBD 32nm SOI design & fabrication flow, which provides:**
  - High-performance library and mixed-signal macros
  - Strategic radiation hardness
  - Single-Event-Effects (SEE) mitigations optimized for power efficiency
  - Assured integrity
• **Employ core competencies of team comprised:**
  - Boeing Solid-State Electronics Development (SSED)
  - Boeing Secure Computing Solutions (SCS)
  - Boeing Space & Launch
  - USC Information Sciences Institute (ISI)
  - University of Michigan ARM Research Center
• **Utilize silicon-proven IP:**
  - ARM, Globalfoundries, Synopsys, Praesum, and Uniquify
• **Leverage tens of millions of dollars of Government and Boeing investments in related technology areas:**
  - DTRA RHBD3, AFRL/NASA Next NGSP, MAESTRO, DARPA PERFECT, etc.
HPSC Chiplet Architecture

HPSC Chiplet
- Boeing Design
- ARM IP
- RHBD Macro
- RHBD RAM
- 3rd Party IP
- Synopsys IP

A53 Cluster 2
- GIC-500
- Clk Gen
- PLL
- NVIC
- Cortex M4F
- Power Mgmt.
- CoreSight
- Clock Mgmt.
- Timers
- Interrupt Mgmt.
- Boot Rom
- 1MB SRAM

A53 Cluster 1
- Quad Cortex A53
- FPU, NEON SIMD
- L1 Cache
- (64KB I, 64KB D)
- 2MB L2 Cache

TRCH
- CoreLink CCN-502
- 4MB L3 Cache
- MMU-500

DRAM CTRL
- DDR3/4 DRAM PHY
- SSTL I/O

NIC-400
- DRAM 330
- DMA 330
- SRI0 EPoInt
- SRI0 EPoInt
- DMA330
- DMA330

EDAC Wrappers
- SMC353
- UART

CMOS
- DDR3/4 Memory
- SRAM/NOR/MRAM
- NAND

Other HPSC Chiplets, FPGA, SpaceVPX, etc.

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Chiplet Architecture: High-performance Cores

Two (2) ARM Cortex-A53 MPCore Clusters

- High-Performance Processing Subsystem (HPPS)
- Four (4) cores per cluster
- ARMv8 64-bit ISA
- Up to 800 MHz frequency
  - Peak 1840 Dhrystone MIPS (DMIPS) per core @ 800MHZ
  - Peak 7360 DMIPS/Quad Cluster, Total of 14,720 DMIPS
- 64 KByte L1 instruction and data cache per core
- 2 MByte L2 Cache per quad cluster
- Floating Point Unit (FPU) per core
- NEON SIMD engine per core
  - 8-bit mode: Peak 12.5 GOPS/NEON, Total 100 GOPS
  - 16-bit mode: Peak 6.25 GOPS/NEON, Total 50 GOPS
  - 32-bit mode: Peak 3.125 GOPS/NEON, Total 25 GOPS
Chiplet Architecture: Interconnect

ARM CoreLink CCN-502

- Cache-coherent ring based interconnect
- AMBA5 Coherent Hub Interface protocol
  - Optimized for ARM v8 64-bit ISA
- 4 MB L3 Cache

- Advanced Power Management Features
- 60 GB/s internal interconnect bandwidth @ 1GHz
- Supports ECC, Quality of Service (QoS), QoS Virtual Networks, and ARM TrustZone security

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Chiplet Architecture: DRAM Interfaces

Two (2) DDR3/4 SDRAM Interfaces for HPPS

- Speeds up to 1600 Megatransfers/second (MT/s)
- Synopsys DDR3/4 Controller
  - Uniquify PHY (uses Boeing RHBD cells)
  - ARM TCZ-400
    - Extends TrustZone security and QoS to external interface
  - Robust ECC allows operation through loss of a whole memory device
  - Provides up to 25.6 GB/s of bandwidth
Six (6) Serial RapidIO® (SRIO) 3.1 ports

- Four (4) lanes per port, each lane up to 10.3125 GBd full-duplex
- Uses Boeing’s 32nm RHBD SerDes macro
- Supports high-speed serial connections to:
  - Other Chiplet devices
  - Expansion FPGA
  - Protocol conversion
- Provides up to 59.1 GB/s of Serial I/O bandwidth

One (1) PCIe Gen2 port dedicated to HPPS

- Uses Boeing’s 32nm RHBD SerDes macro (2 lanes)
- Synopsys PCIe Controller
- 1 GB/s Bandwidth
Chiplet Architecture: TRCH Controller

**Timing, Reset, Config, & Health (TRCH) Controller**

- Built around a small Cortex-M4F microcontroller
  - Low power and small form factor
  - More flexibility than a finite state machine approach
  - TMRed for maximal fault tolerance
  - 1 MB Tightly-Coupled Memory (TCM) SRAM with Double-Error Correct, Triple-Error Detect (DECTED) ECC

Provides the following Chiplet functionality:

- Boot Sequencing
- Power-On-Reset
- Clock Generation
- Power Management
- Configuration Control
- Sleep Mode (< 50mW)
- Health Monitoring / Fault Management
- Built-in-Self-Test, eFuse
- Timers and Synchronization Control
- Interrupt handling and distribution

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Chiplet Architecture:
Realtime Processing Subsystem

Realtime Processing Subsystem (RTPS)

- Single Cortex-A53 core managing two (2) Cortex-R52 Realtime cores (ARM v8 64b)
  - Supports virtualization and time & space partitioning / ARINC 653, as well as realtime performance needs

- RTPS Dedicated Memory & IO interfaces:
  - One (1) DDR3/4 interface
  - One (1) PCIe Gen2 interface
  - One (1) SPI interface

- R52 cores provide:
  - ARM’s highest level of safety features, including Dual-Core Lock Step (DCLS) operation
  - Up to 600 MHz frequency
  - Peak 1296 Dhrystone MIPS (DMIPS) per core @ 600MHZ
  - Floating Point Unit (FPU), NEON SIMD engine, and 1 MB Tightly Coupled Memory per core

- A53 core provides:
  - Peak 1380 Dhrystone MIPS (DMIPS) @ 800MHZ
  - 32 KB L1, 256 KB L2 Caches
Chiplet Architecture: Other IO Interfaces

- Two (2) 10/100/1000 Ethernet Interfaces
- 3-Port Time-Triggered Ethernet (TTE) interface
  - Can operate as a single TMRed port for fault tolerance
- 2-Port Spacewire Interface
- UART, SPI, and I²C interfaces
- SRAM and NVRAM (NAND/NOR Flash, MRAM) interfaces
- ARM CoreSight trace and debug, JTAG debug interfaces
- GPIO (single-ended and LVDS)
Performance @ Power Predictions

HPSC Chiplet Performance at Power

Scenario 1
9-15 GOPS* in
7-10 Watts with
50% IO Utilization
50% Memory Utilization

Scenario 2
0.3 - 1 GOPS* in
0.5-1.0 Watts with
10% IO Utilization
10% Memory Utilization

Scenario 3
Sleep Mode
100 mW

HPSC Chiplet Performance, Power, and Fault Tolerance Scalability

* GOPS not including SIMD engine performance

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• The HPSC Chiplet inherits a large complement of existing open source software including:
  ▪ Libraries, operating systems, compilers, and debuggers.
• We’re able to leverage much of this software unmodified.
• The HPSC System Software effort largely encompasses 4 thrusts:
  1. Board support packages for Linux and RTOS;
  2. Development tools (e.g., compilers, debuggers, IDEs);
  3. Software-based fault tolerance; and
  4. Chiplet emulators.
• Our goal is to build a sustainable software ecosystem to enable full lifecycle software development.
• AFRL is funding JPL and NASA GSFC to develop HPSC Middleware

• Middleware will provide a software layer that provides services to the higher-level application software to achieve:
  - Configuration management
  - Resource allocation
  - Power/performance management
  - Fault tolerance capabilities of the HPSC chiplet

• Serving as a bridge between the upper application layer and lower operating system or hypervisor, the middleware will significantly reduce the complexity of developing applications for the HPSC chiplet

INTEGRATED STACK CONCEPT

Mission Applications

FSW Product Lines – Core S/C Bus Functions
GSFC and JPL Core Flight Software (CFS)

HPSC Middleware – Resource Management
Mission-Friendly Interface for Managing/Allocating Cores for Performance vs. Power vs. Fault Tolerance

Traditional System Software – RTOS or Hypervisor, FSW Development Environment

Hardware – Multi-core Processor Chips, Evaluation Boards
HPSC Use Cases – Rovers and Landers

**Rover**

**Compute Needs**
- Vision Processing
- Motion/Motor Control
- GNC/C&DH
- Planning
- Science Instruments
- Communication
- Power Management
- Thermal Management
- Fault detection/recovery

**System Metrics**
- 2-4 GOPs for mobility (10x RAD750)
- >1 Gb/s science instruments
- 5-10 GOPs science data processing
- >10 KHz control loops
- 5-10 GOPS, 1 GB/s memory BW for model based reasoning for planning

**Lander**

**Compute Needs**
- Hard Real time compute
- High rate sensors w/zero data loss
- High level of fault protection/fail over

**System Metrics**
- >10 GOPs compute
- 10 Gb/s+ sensor rates
- Microsecond I/O latency
- Control packet rates >1 Kpps
- Time tagging to microsecond accuracy

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HPSC Use Cases - High Bandwidth Instruments and SmallSats/Constellations

High Bandwidth Instrument

Compute Needs
- Soft real time
- Non-mission critical
- High rate sensors
- Large calibration sets in NV memory

System Metrics
- 10-20 GOPs compute
- >10GB/s memory bandwidth
- >20Gbps sensor IO data rates

Smallsat

Compute Needs
- Hard and Soft real time
- GNC/C&DH
- Autonomy and constellation (cross link comm)
- Sensor data processing
- Autonomous science

System Metrics
- 2-5Gbps sensor IO
- 1-10GOPS
- 1GB/s memory bandwidth
- 250Mbps cross link bandwidth

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Similar to Orion’s two fault tolerant architecture:

- A single HPSC exceeds the performance metrics of a Orion Vehicle Management Computer (VMC)
- A VMC contains three Self-Checking Pairs (SCP)
Broader HPSC Ecosystem

• Beyond the HPSC Chiplet, System Software, and Middleware developments, further investments can implement a robust HPSC avionics ecosystem

  ▪ Advanced Spaceflight Memory
  ▪ Increased RTOS Support
  ▪ Multi-Output Point-Of-Load Converters
  ▪ Coprocessors (GPU, Neuromorphic, etc.)
  ▪ Special Purpose Chiplets (Security Chiplet, etc.)
  ▪ Advanced Packaging (Multiple Chiplets in a Package)
  ▪ Single Board Computers
Conclusion

• As illustrated by the NASA use cases, our future missions demand the capabilities of HPSC

• Improved spaceflight computing means enhanced computational performance, energy efficiency, and fault tolerance

• With the ongoing HPSC development, we are well underway to meeting future spaceflight computing needs

• The NASA-developed Middleware will allow the efficient infusion of the HPSC chiplet into those missions

• Further investments can implement a full HPSC avionics ecosystem

Acknowledgements: Rich Doyle (JPL), Rafi Some (JPL), Jim Butler (JPL), Irene Bibyk (GSFC), Jonathan Wilmot (GSFC), and Jon Ballast (Boeing) for diagrams and use case definitions