Abstract. The direct-current (DC) electrical behavior of n-type 4H-SiC resistors used for realizing 500 °C durable integrated circuits (ICs) is studied as a function of substrate bias and temperature. Improved fidelity electrical simulation is described using the SPICE NMOS model to simulate resistor substrate body-bias effect which is absent from the SPICE semiconductor resistor model.

1. Background
Increasingly capable extreme-temperature-durable 4H-SiC JFET ICs are being demonstrated.

2. Body-Bias Effect
As shown below in Fig. 4, the cross-sectional illustration of the SiC resistor structure used to realize the above JFET IC's, bias-dependent substrate pn junction depletion affects undepleted thickness (and therefore conductivity) of the resistor n-channel.

- Experimental SiC fabrication, packaging, and measurement setup are described in [2–5].
- For applied resistor bias $V_R > 0$, depletion widths change across the lateral length of the resistor.
- Current vs. voltage (I-V) characteristics and the IC resistor resistance value depend on both $V_R$ and $V_V$.

3. Measured Impact of Body Bias Effect on Resistor I-V Characteristics
- Body-bias effect causes mild non-linearity (i.e., downward bending) of resistor I-V characteristics (shown in green).
- Amount of non-linearity can be quantified by plotting differential resistance $R_{diff} = dV/dI$ (shown in blue).

4. Resistor SPICE Model With Body Effect
While Fig. 4 depicts a SiC IC resistor cross section, this resistor structure can also be considered a long-channel JFET with the electrically biased p-epilayer/substrate serving as the gate terminal.
- The resistor can therefore be modeled using the SPICE NMOS LEVEL=1 model [6].
- The magnitude of negative substrate voltage $V_V$ required to completely deplete the n-channel is large since NAS << NDC (Fig. 4), so the JFET operates in the linear region as a substrate-bias controlled resistor.
- The SPICE NMOS LEVEL=1 parameters for modeling IC resistors as N-MOSFETs with body bias effect (such as in green text SPICE listings shown below) can be extracted from Fig. 5 I-V data using the low drain-bias NMOS parameter extraction procedure described in [7].

5. Conclusion
For improved accuracy circuit design and modeling of 4H-SiC JFET ICs using SPICE, the NMOS resistor modeling approach described in this report should supercede/replace the standard SPICE R resistor model reported in [6], which ignores the body-bias effect.

6. Future Work
Comparison and design studies of SiC JFET integrated circuits using new SPICE NMOS resistor modeling.

7. Acknowledgements

8. References